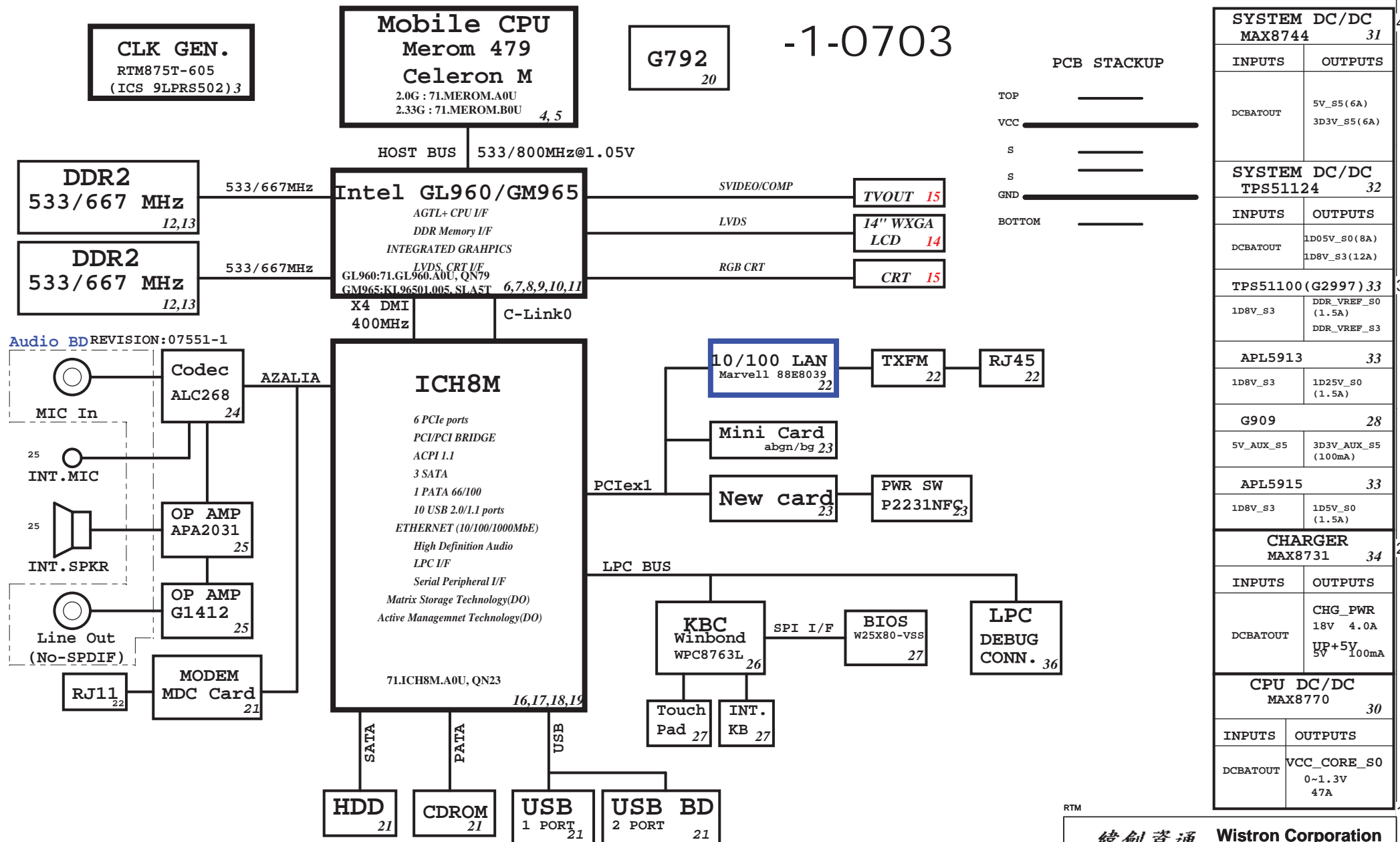


# Volvi2 Block Diagram

Project code: 91.4X101.001  
PCB P/N : 48.4X101.011  
REVISION : 07220-1

-1-0703



REVISION:07570-1

RTM

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series

Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCIE Routing

LANE1	LAN Marvell
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	NC
6	NC
7	MINICARD
8	CCD
9	NEW1

ICH8M Integrated Pull-up  
and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K ?
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K ?
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

2007/05/02  
1 Based on Tahoe to modify schematics.  
=====

2007/05/14  
1. Page 34: Replace "D25" with "BAS16-1-GP".  
2. Page 27: Replace "R485" with "2K7R2j".  
3. Page 27: DY: C379"  
4. Page 27: Add "C682" Dlu capacitor on "LID1.PIN1"  
5. Page 27: Replace "R238" with "OR2".  
6. Page 25: Replace "INTMIC1" & "SPKR1" with main source follow connector list.  
7. Page 5: Add C115, C116, C141, C149, C169, C171 for Colay with TC25.  
8. Page 10: Replace "L20" with "68.00217.141".  
9. Page 10: Replace "L10" & "L23" with "68.00217.101"  
=====

Crestline Strapping Signals and  
Configuration

Crestline EDS 20954 1.0

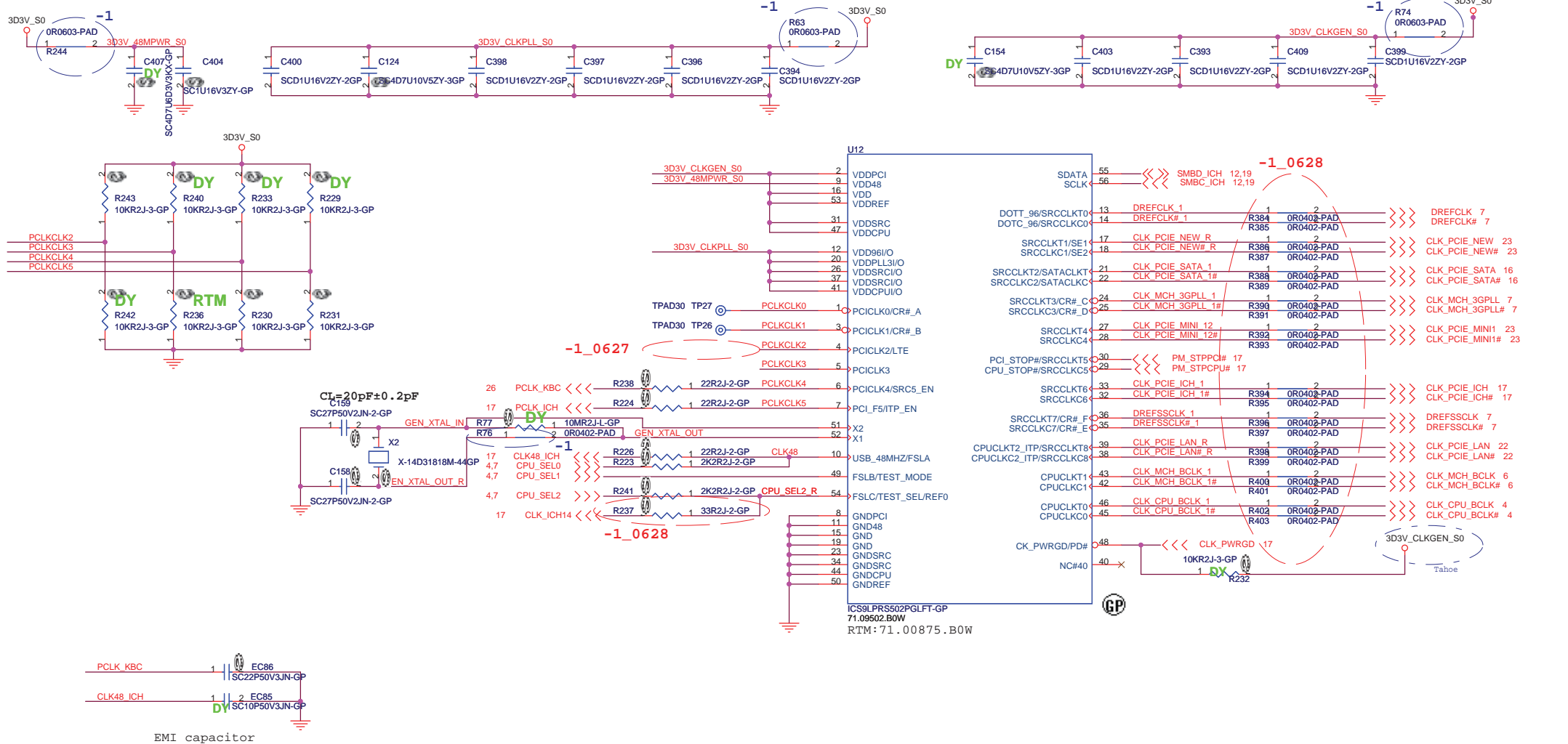
page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation(Default): Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default): lane Numbered in order 1 =Reverse Lane, 4->0, 3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading  
edge of the Crestline GMCH PWORK in signal.

RTM

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Title		
Reference		
Size A3	Document Number	Rev -1
Date: Thursday, July 05, 2007		
Sheet 2 of 36		



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRCB/SRCB# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRCB/SRCB# 1 = ITP/ITP#

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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Taipei Hsien 221, Taiwan, R.O.C.

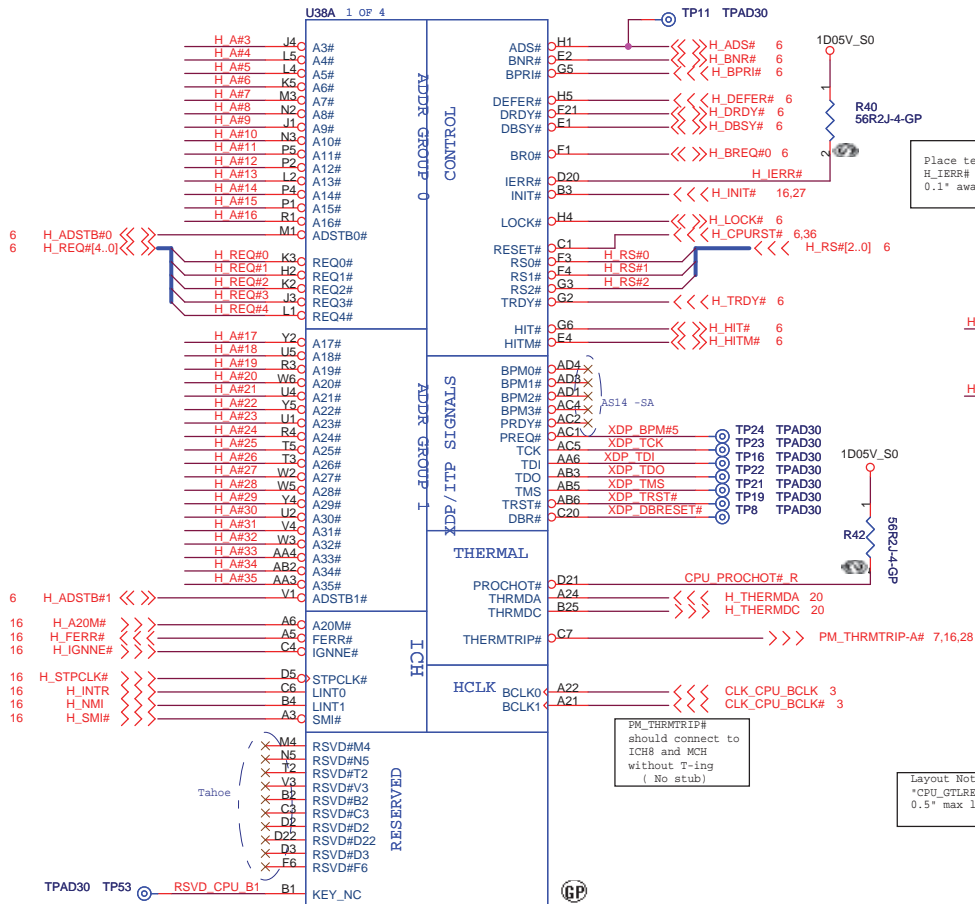
Title  
Clock Generator

Size Document Number  
Volvi2

Rev  
-1

Date: Thursday, July 05, 2007 Sheet 3 of 36

6 H\_A#(35..3) <<>> H\_A#(35..3)



Place testpoint on H\_IERR# with a GND 0.1" away



Layout Note:  
"CPU\_GTLREF0"  
0.5" max length.

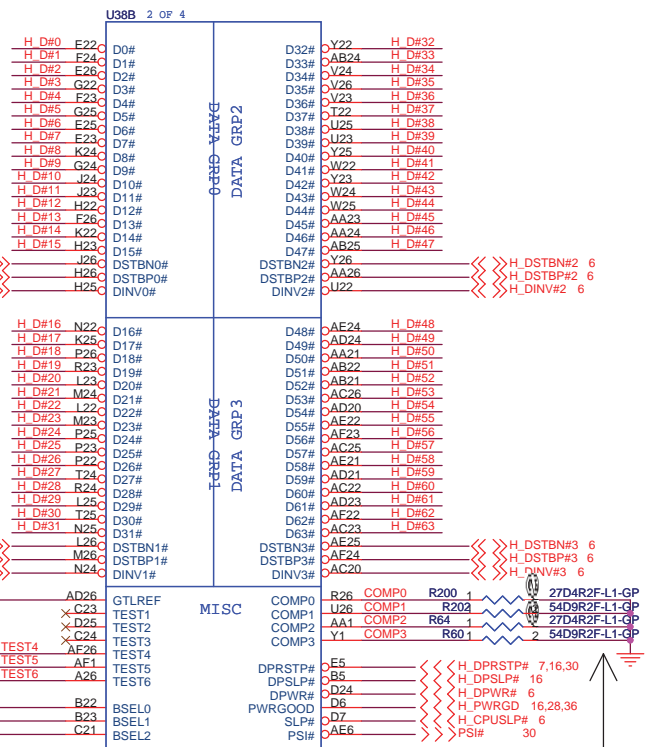
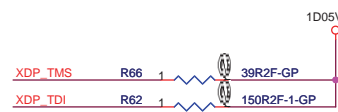
PM\_THRMTRIP#  
should connect to  
ICH8 and MCH  
without T-ing  
(No stub)

CPU\_GTLREF0

TPAD30 TP25  
TPAD30 TP6  
TPAD30 TP7

3.7 CPU\_SEL0  
3.7 CPU\_SEL1  
3.7 CPU\_SEL2

Net "TEST4" as short as possible,  
make sure "TEST4" routing is  
reference to GND and away other  
noisy signals

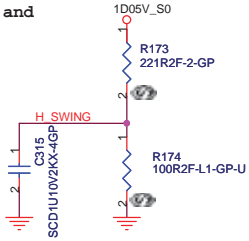


Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make  
trace length shorter than 0.5"  
Comp1, 3 connect with Zo=55 ohm, make  
trace length shorter than 0.5"

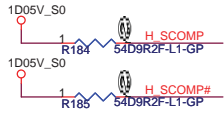


H\_SWING routing Trace width and Spacing use 10 / 20 mil

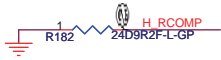
H\_SWING Resistors and Capacitors close MCH 500 mil ( MAX )



H\_SCOMP and H\_SCOMP# Resistors and Capacitors close MCH 500 mil ( MAX )

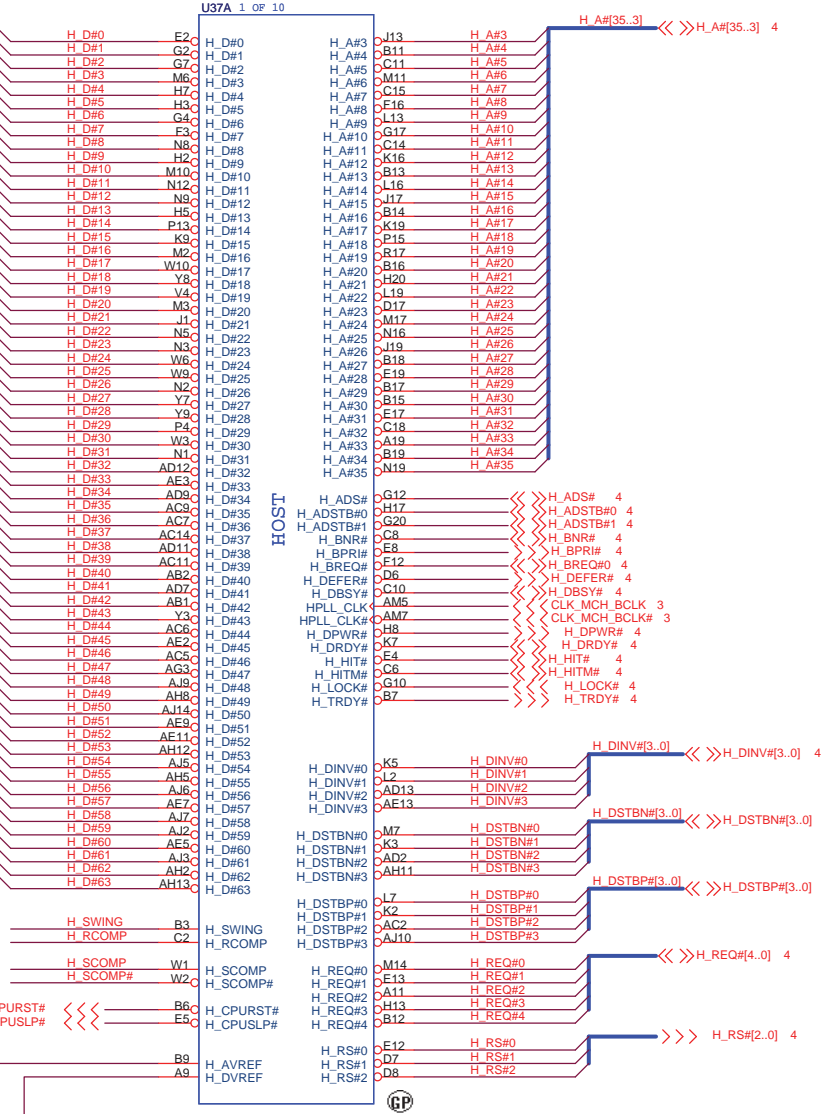
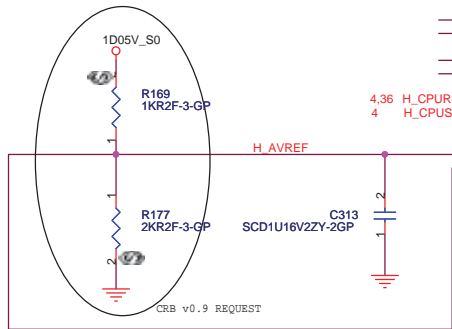


H\_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip ( < 0.5")

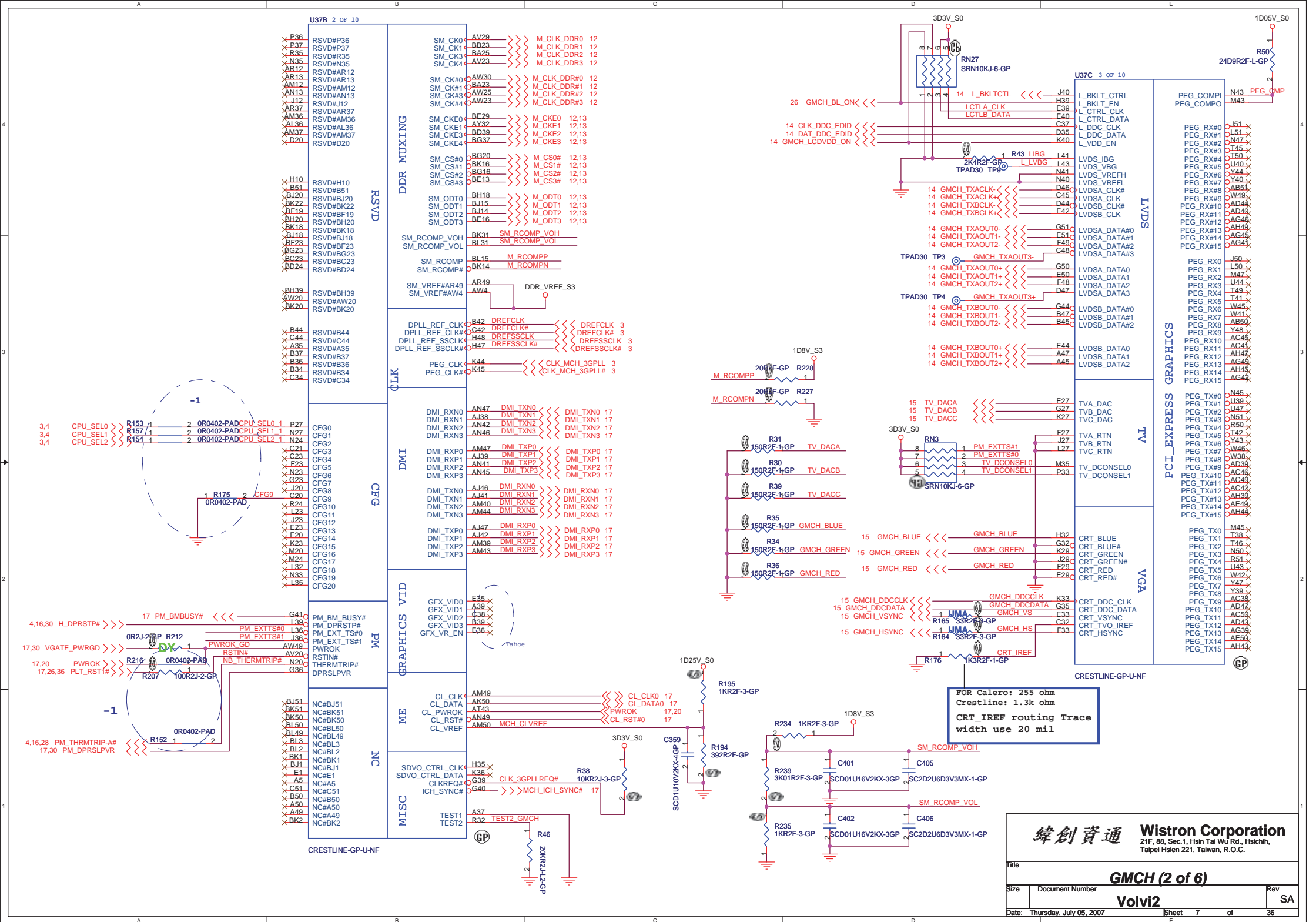
H\_REF Decoupling Crestline close Crestline 100 mil

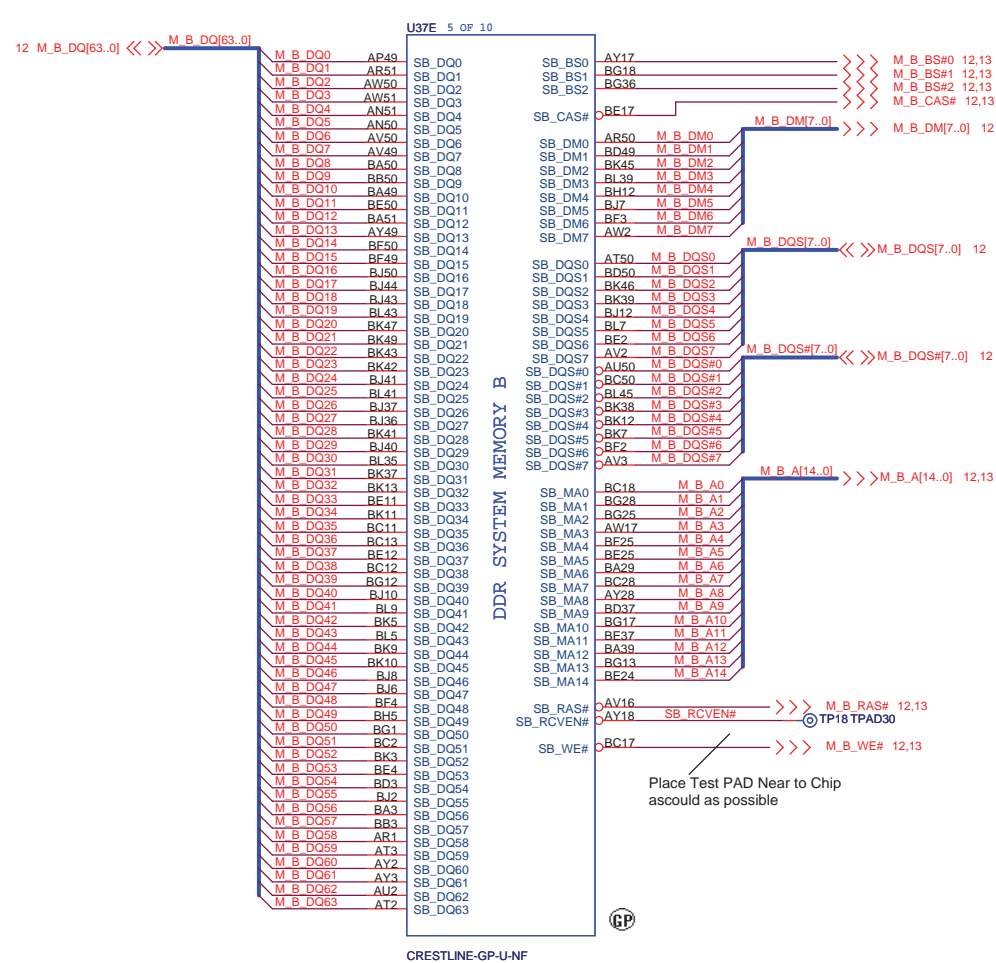
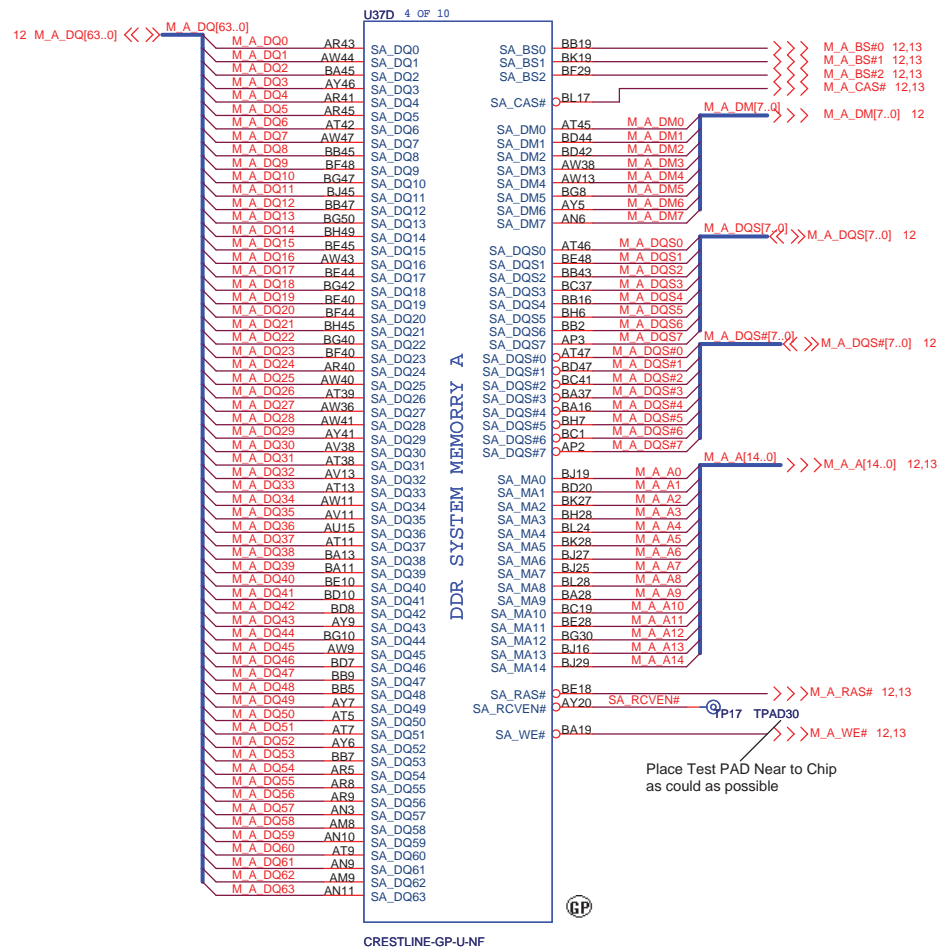


RTM

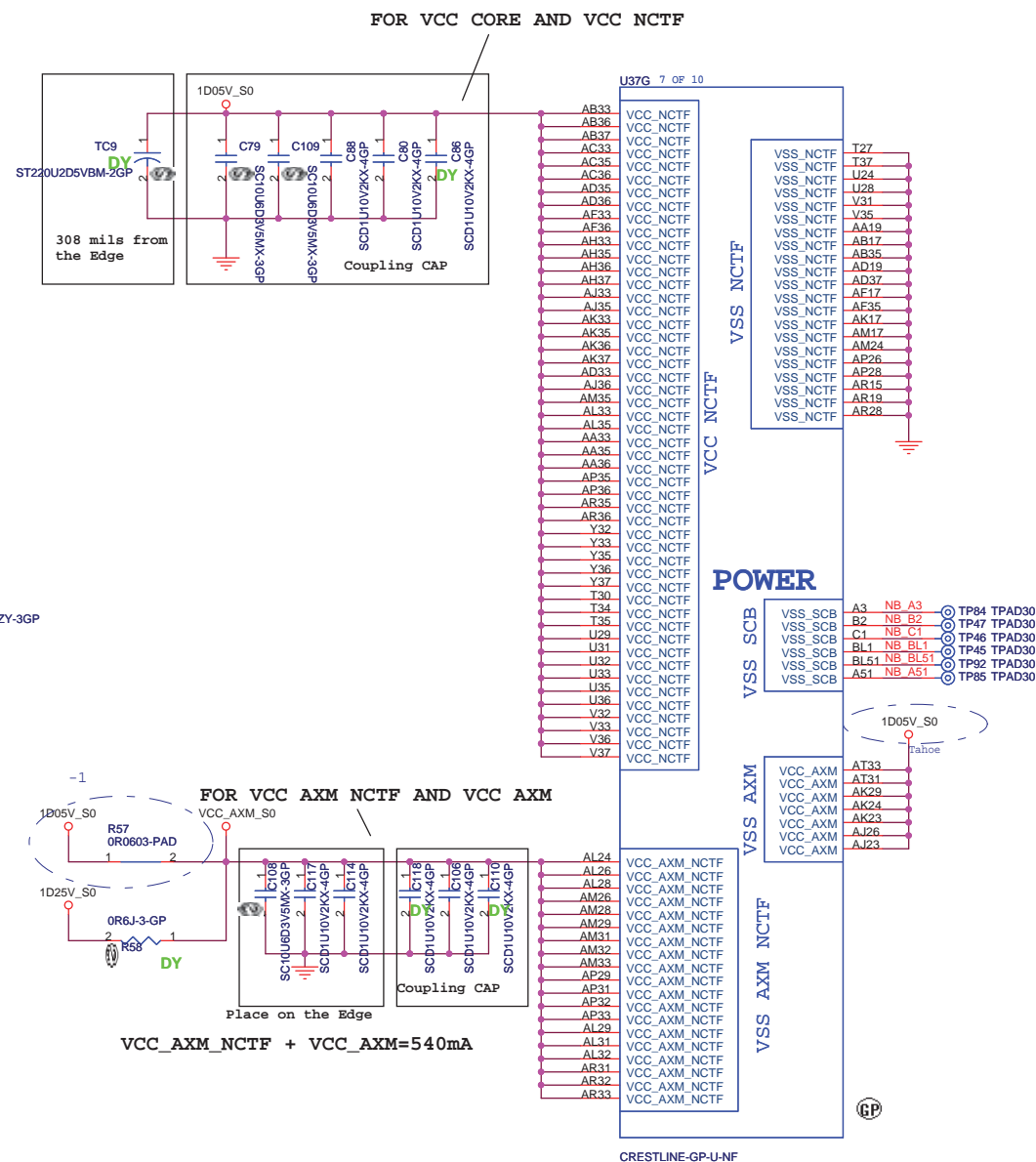
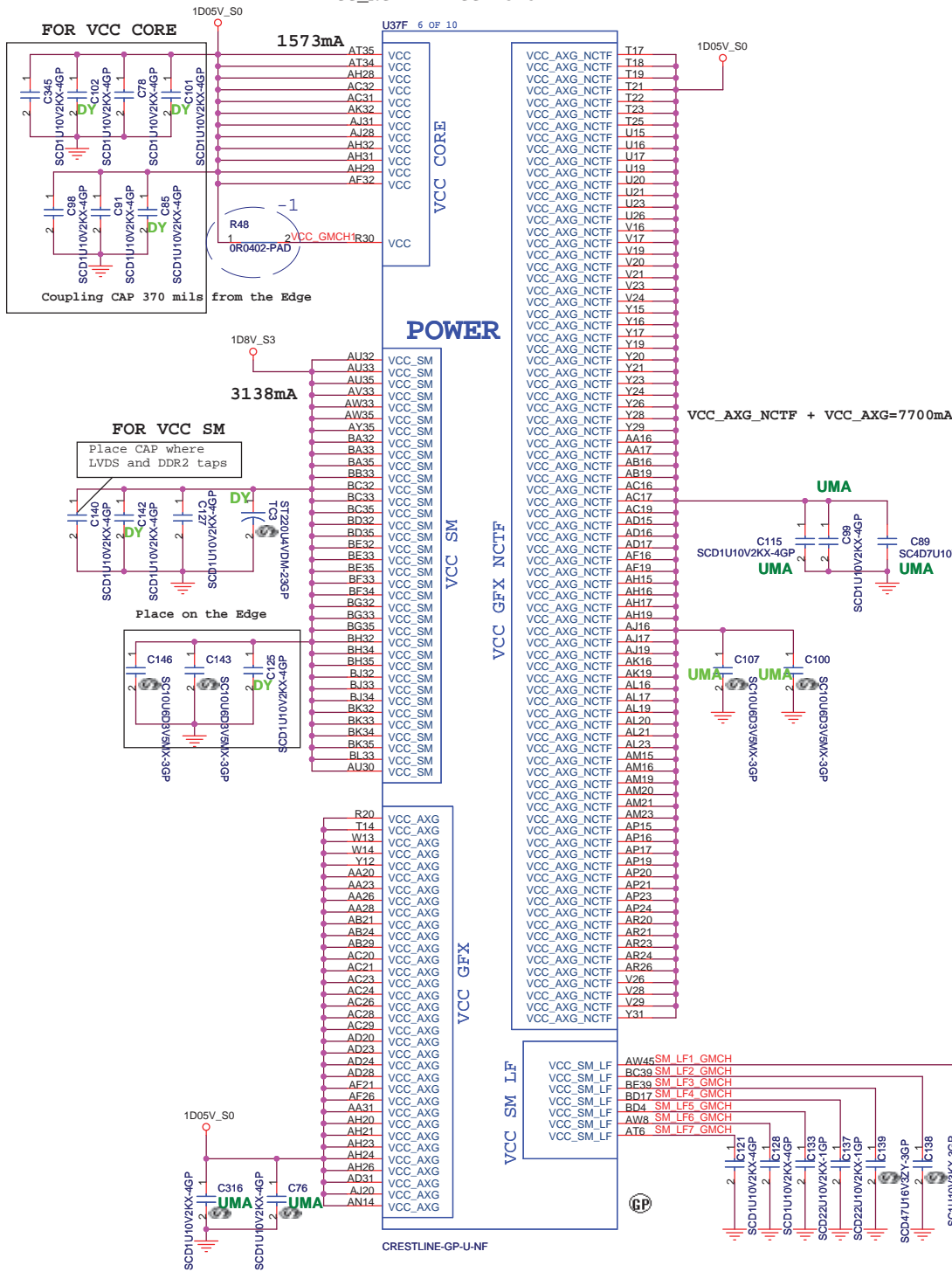
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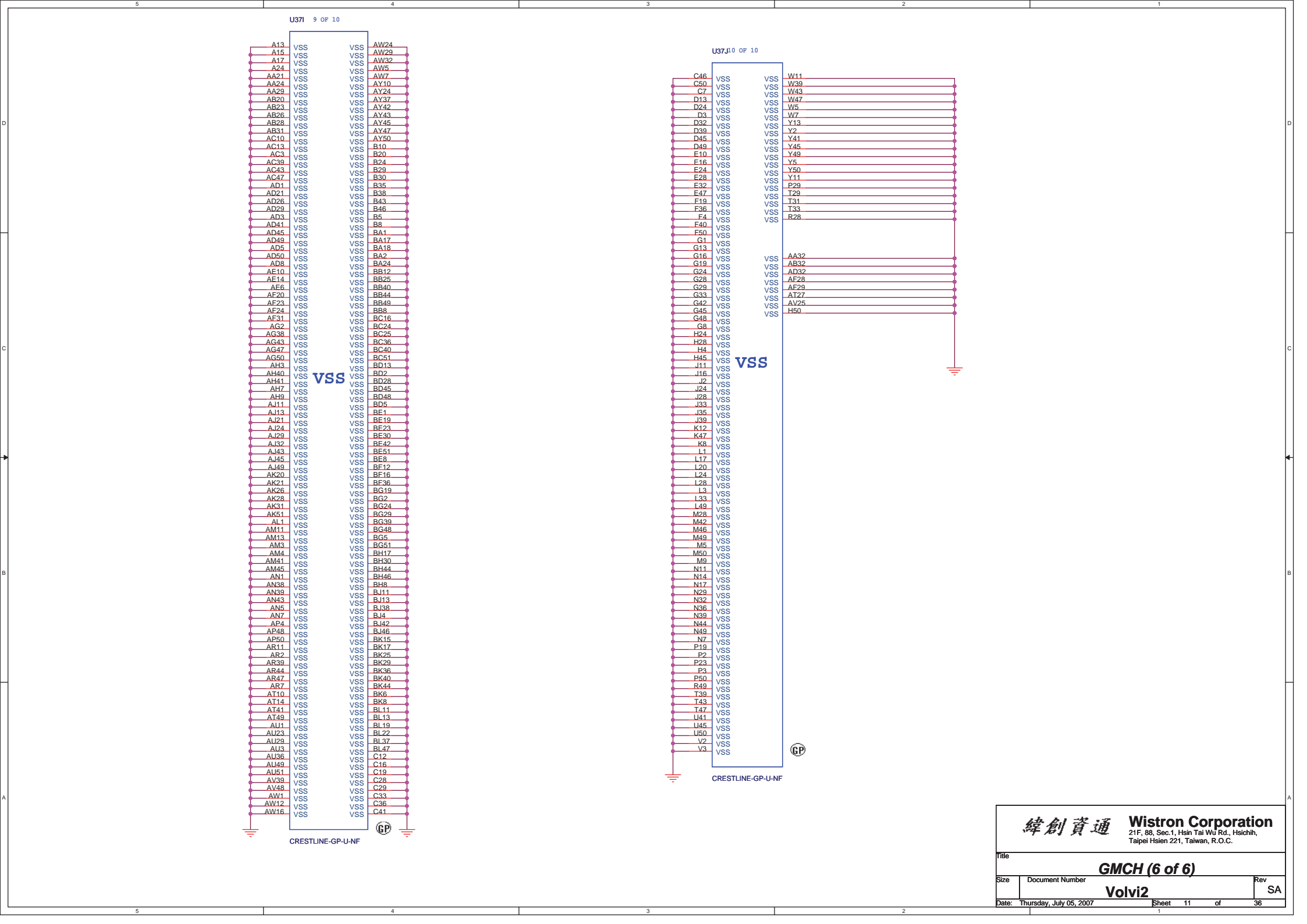


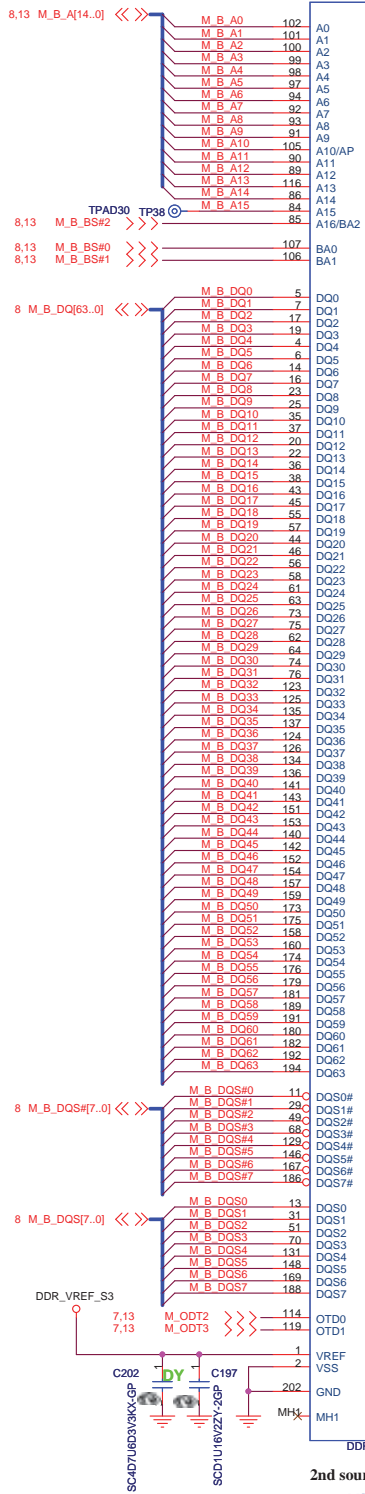




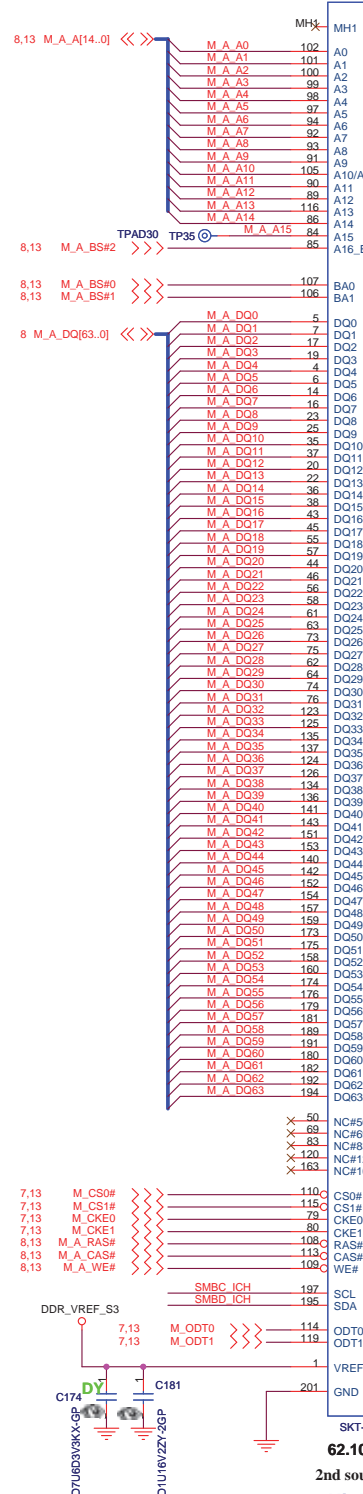
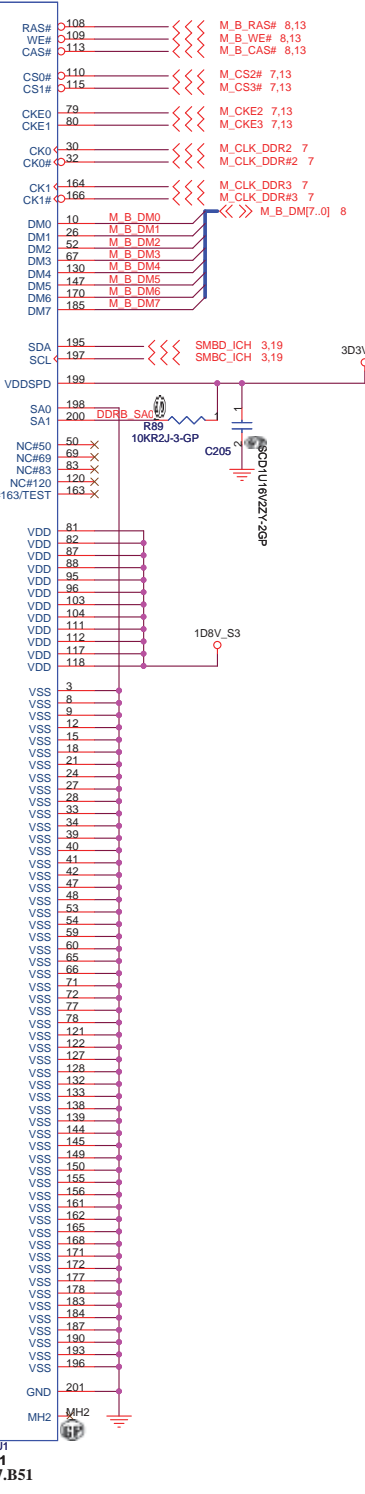




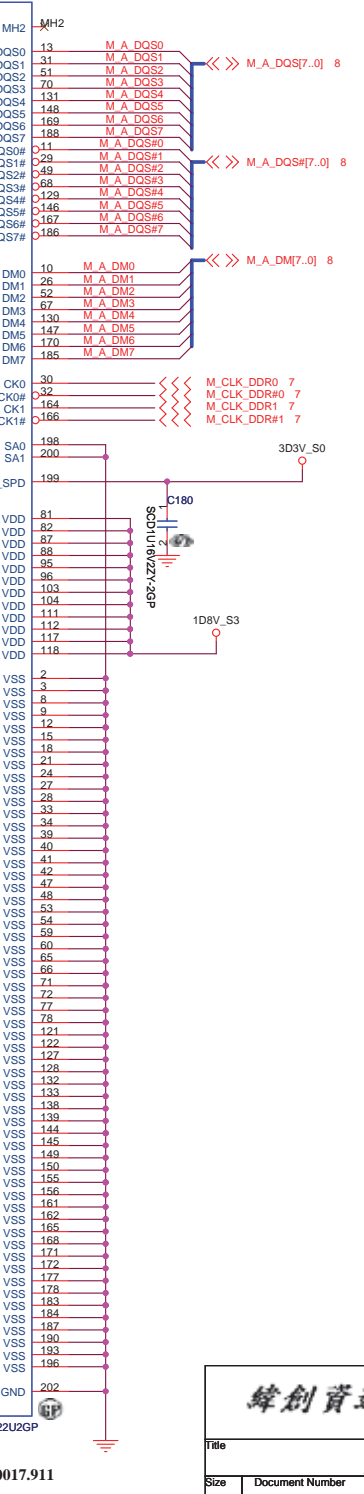




REVERSE TYPE



REVERSE TYPE



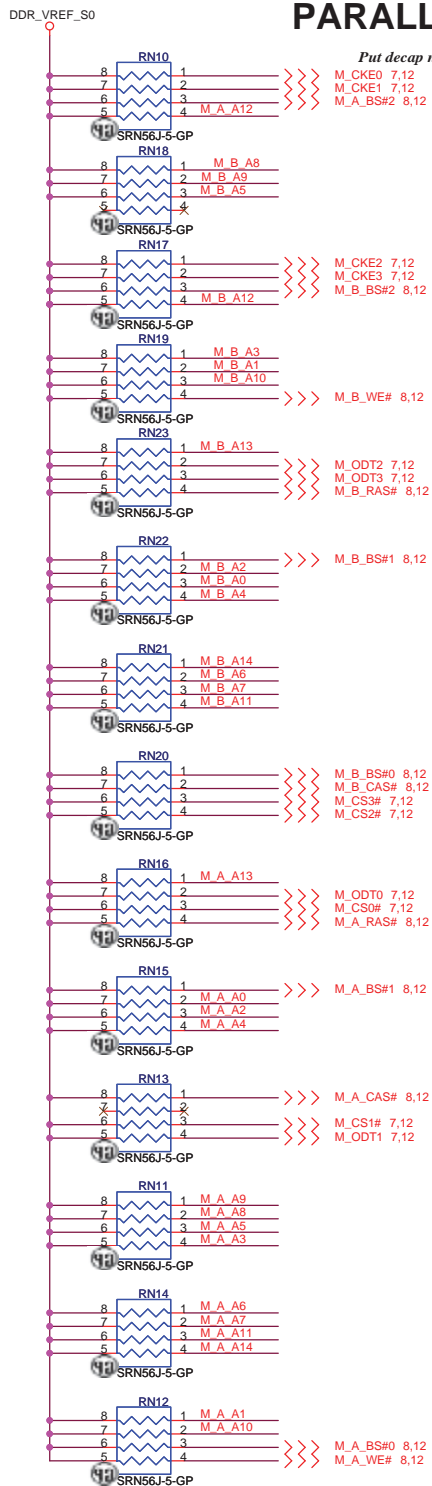
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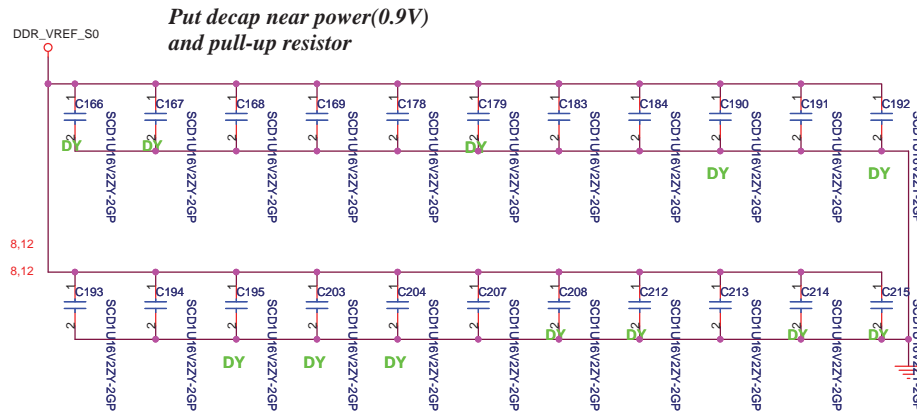
Title	DDR2 Socket		
Size	Document Number	Rev	SA
Date: Thursday, July 05, 2007		Sheet 12 of 36	

# PARALLEL TERMINATION

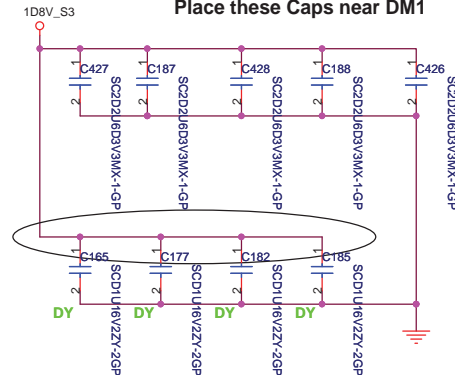


M\_A\_A[14..0] << M\_A\_A[14..0] 8,12  
M\_B\_A[14..0] << M\_B\_A[14..0] 8,12

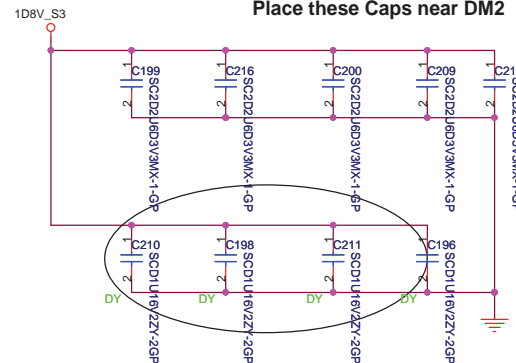
# Decoupling Capacitor



## Place these Caps near DM1



## Place these Caps near DM2



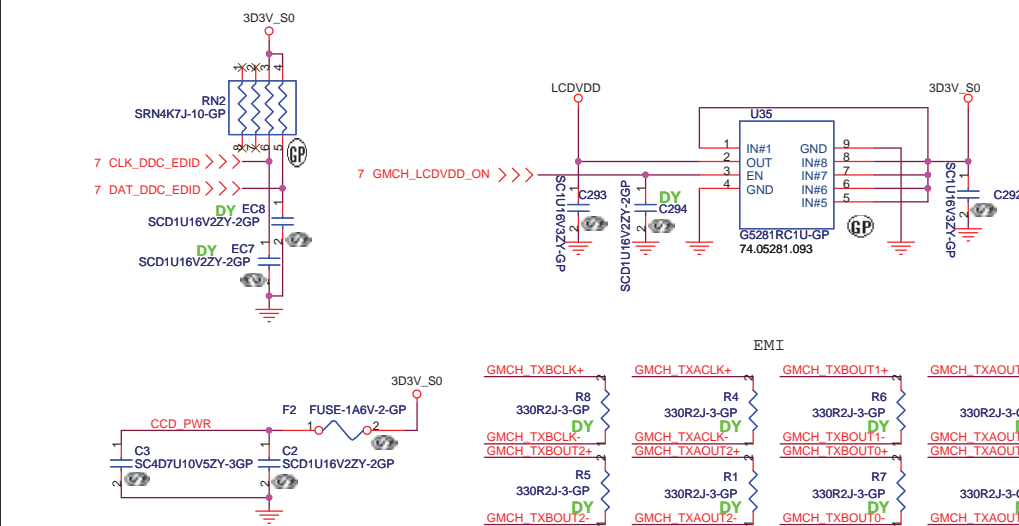
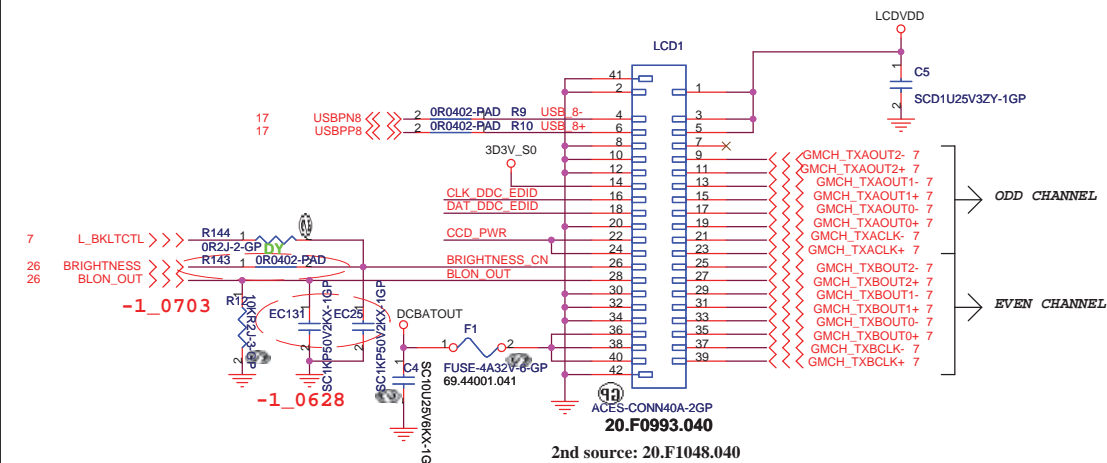
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Title			
DDR2 Termination Resistor			
Size	Document Number		Rev
	Volvi2		SA
Date: Thursday, July 05, 2007	Sheet 13	of 36	

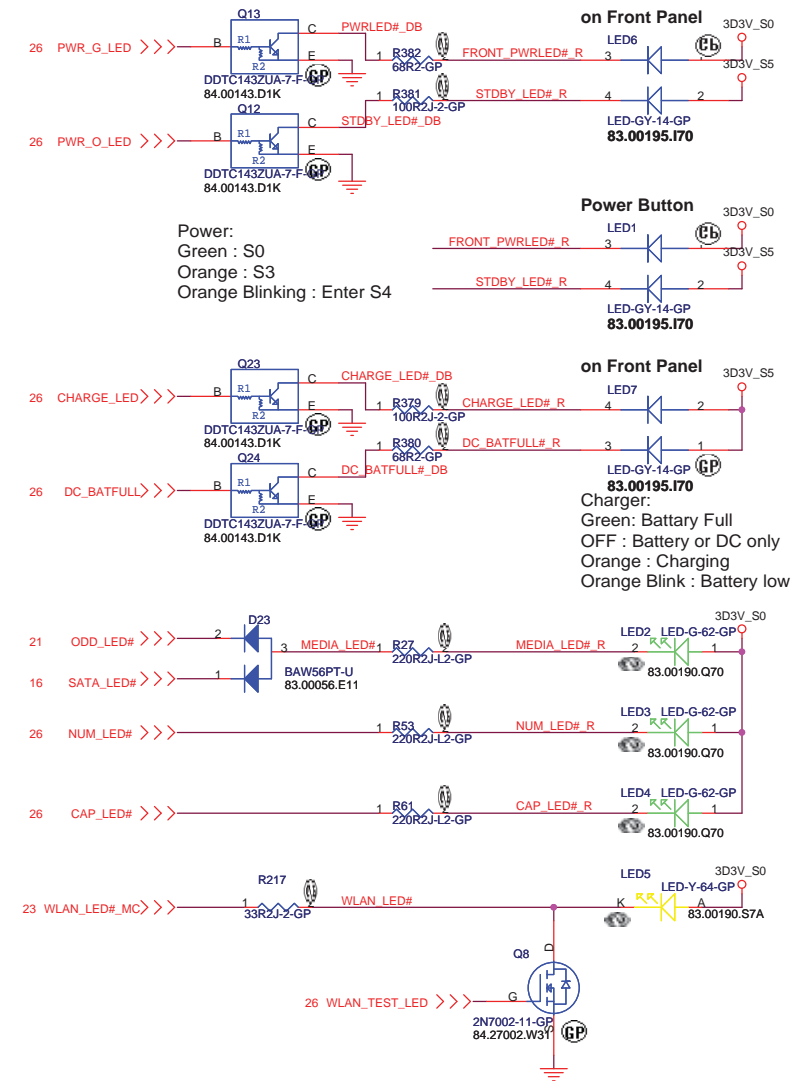
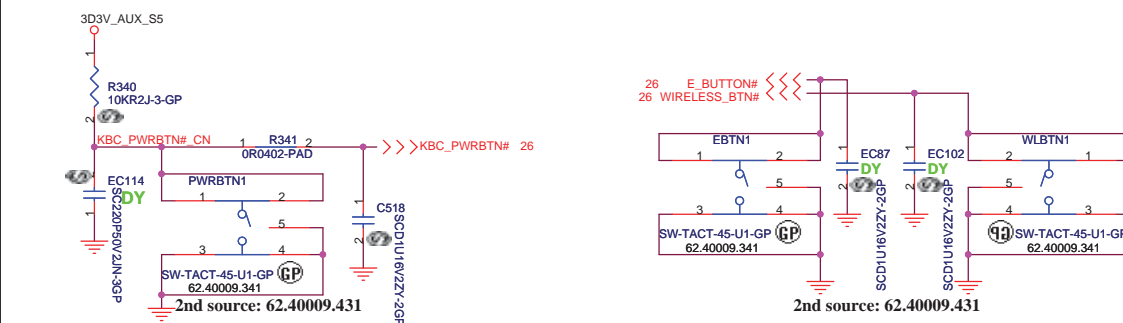


# LCD/INVERTER CONN

# LED



# Buttons



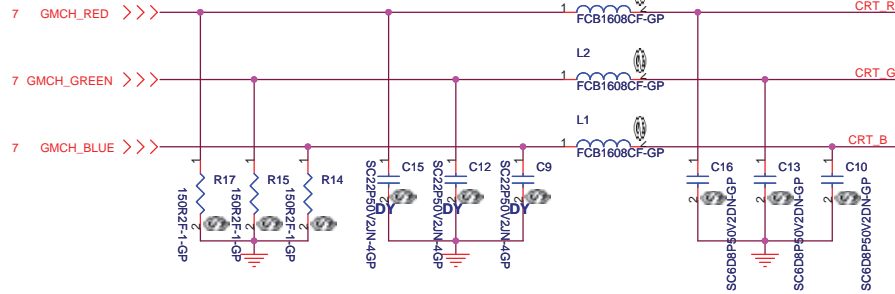
RTM

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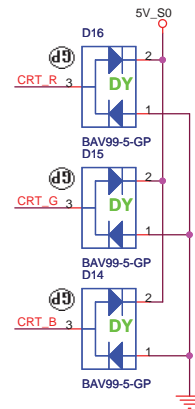
LCD CONN & LED & Buttons			
Size	Document Number	Volvi2	Rev SA
Date: Thursday, July 05, 2007	Sheet 14	of	36

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

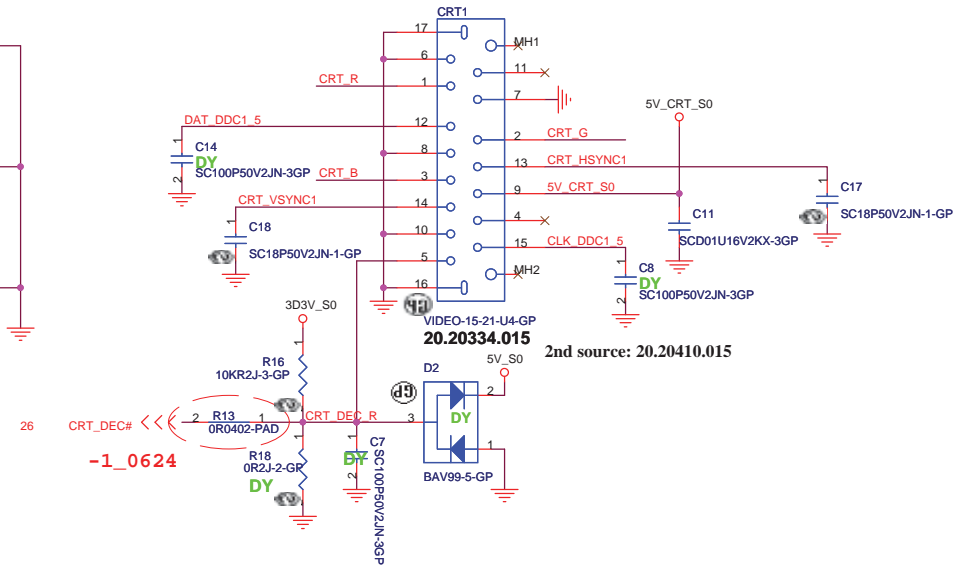
Ferrite bead impedance: 10 ohm@100MHz



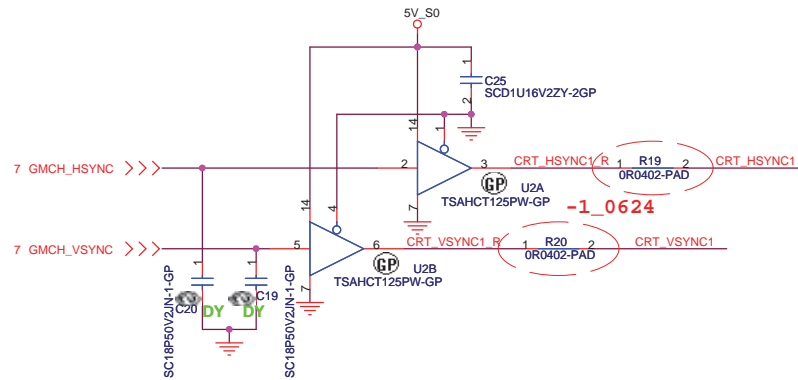
**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



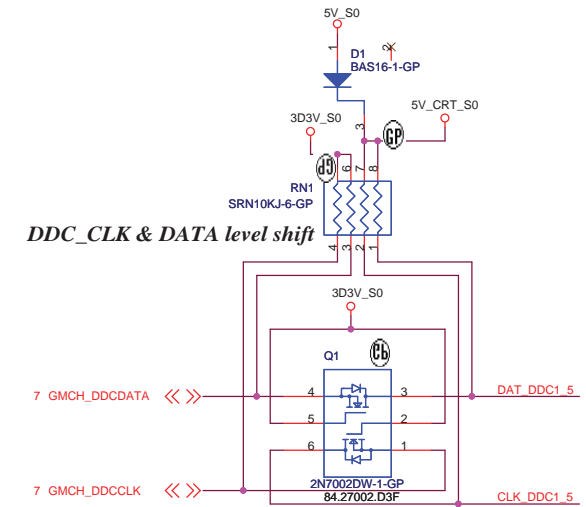
## CRT I/F & CONNECTOR



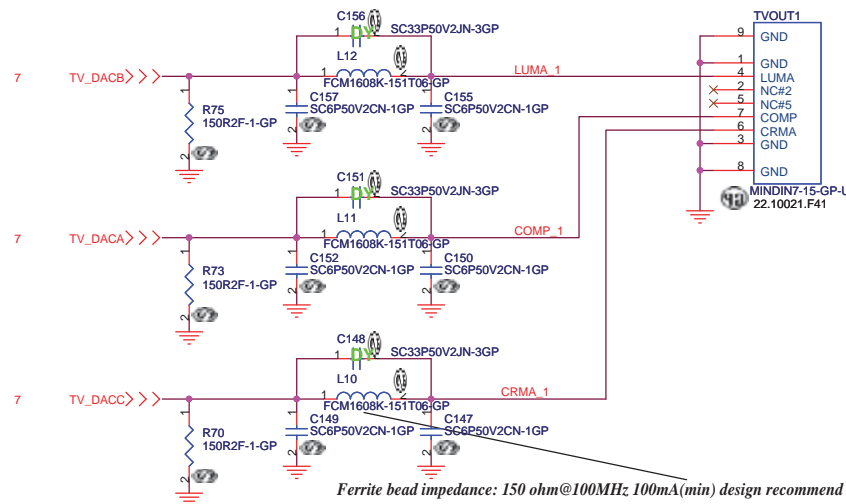
### Hsync & Vsync level shift



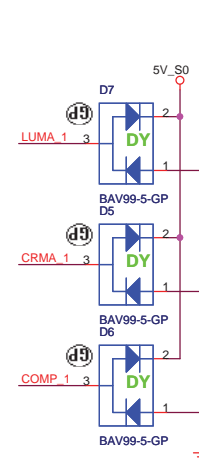
### DDC\_CLK & DATA level shift



## TV CONN

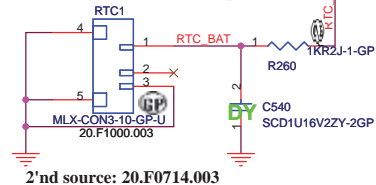


Ferrite bead impedance: 150 ohm@100MHz; 100mA(min) design recommend

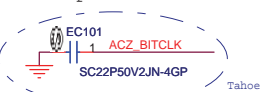


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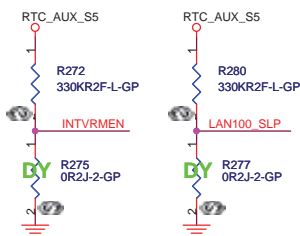
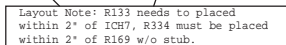
Title				CRT/TV Connector			
Size	Document Number					Rev	SA
Volvi2							
Date:	Thursday, July 05, 2007			Sheet	15	of	36



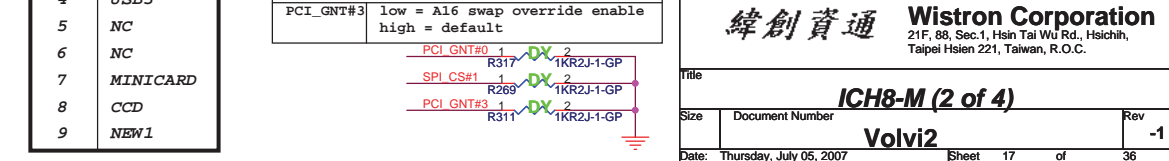
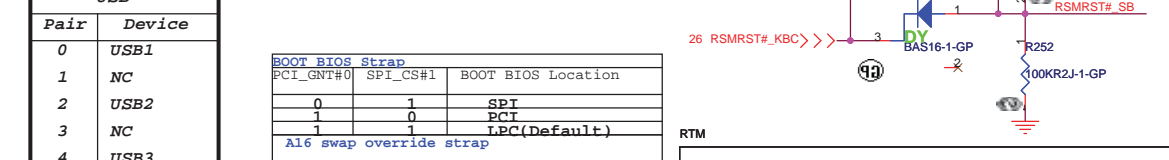
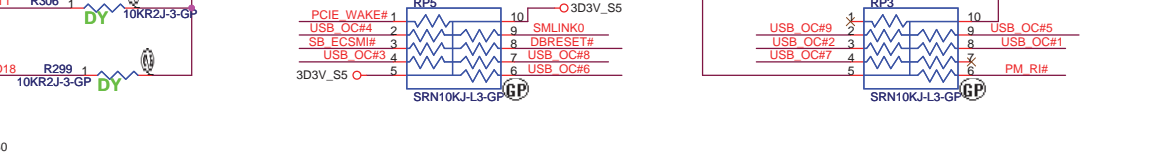
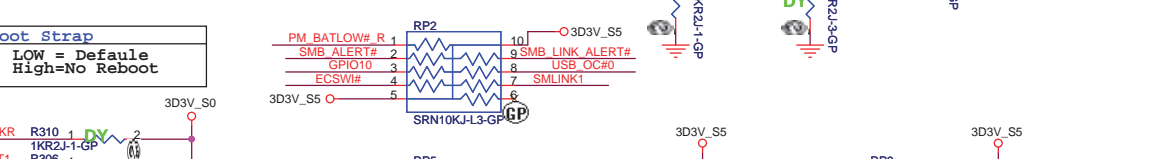
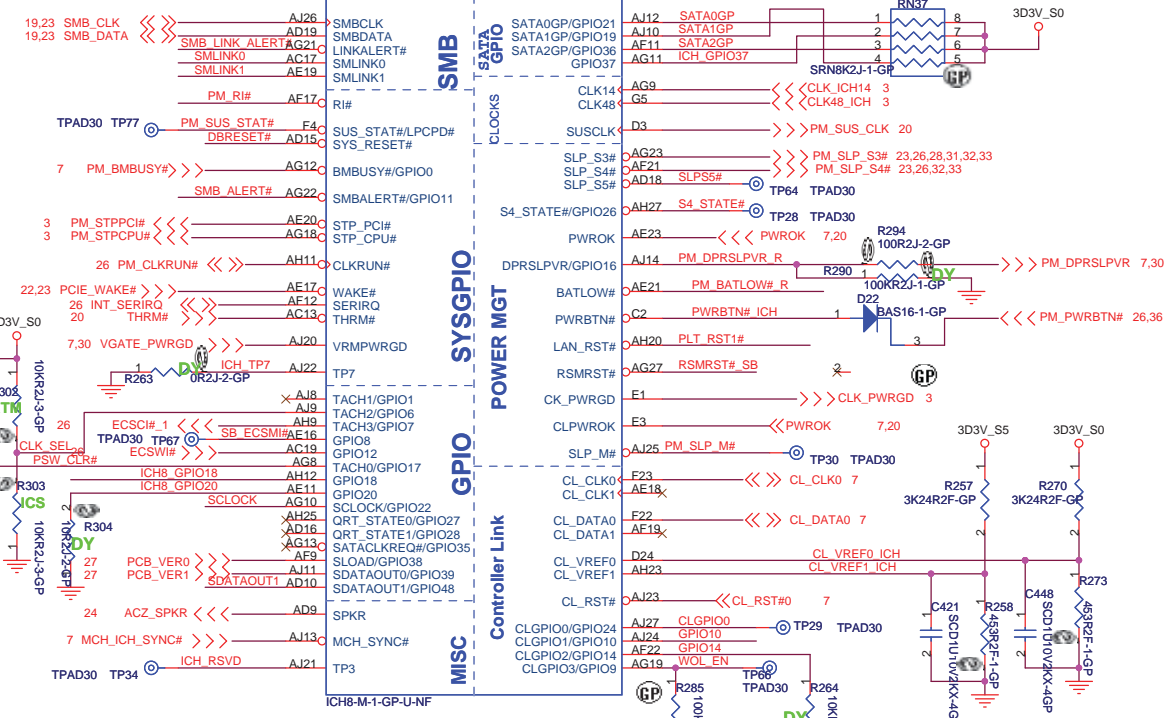
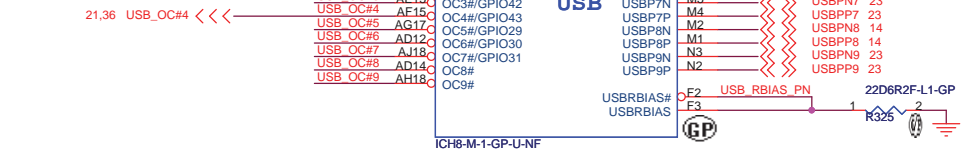
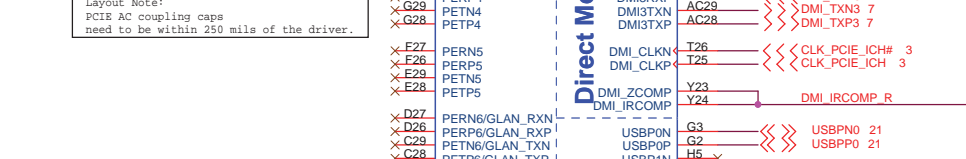
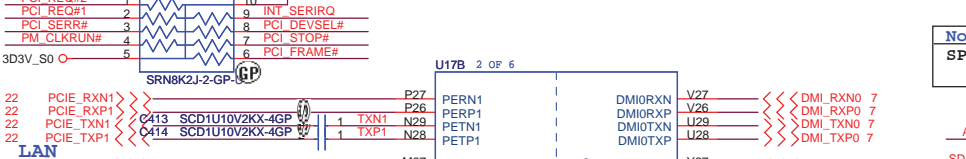
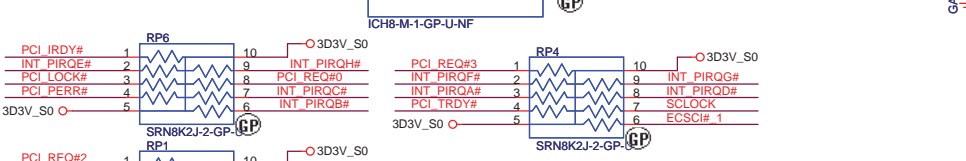
2'nd source: 20.F0714.003



## Tahoe



integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable



No Reboot Strap  
SPKR LOW = Default  
High = No Reboot

# USB Table

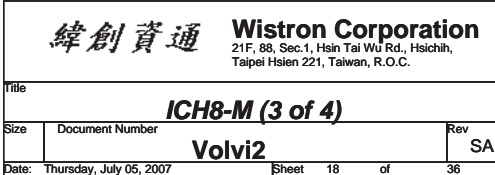
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	NC
6	NC
7	MINICARD
8	CCD
9	NEW1

Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	NC
6	NC
7	MINICARD
8	CCD
9	NEW1

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ICH8-M (2 of 4)  
Volvi2

File: \_\_\_\_\_  
Size: \_\_\_\_\_ Document Number: \_\_\_\_\_ Rev: -1  
Date: Thursday, July 05, 2007 Sheet 17 of 36

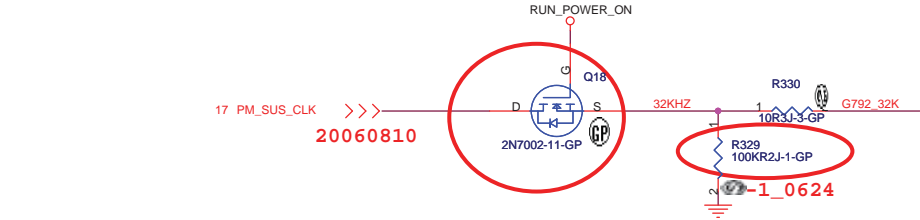
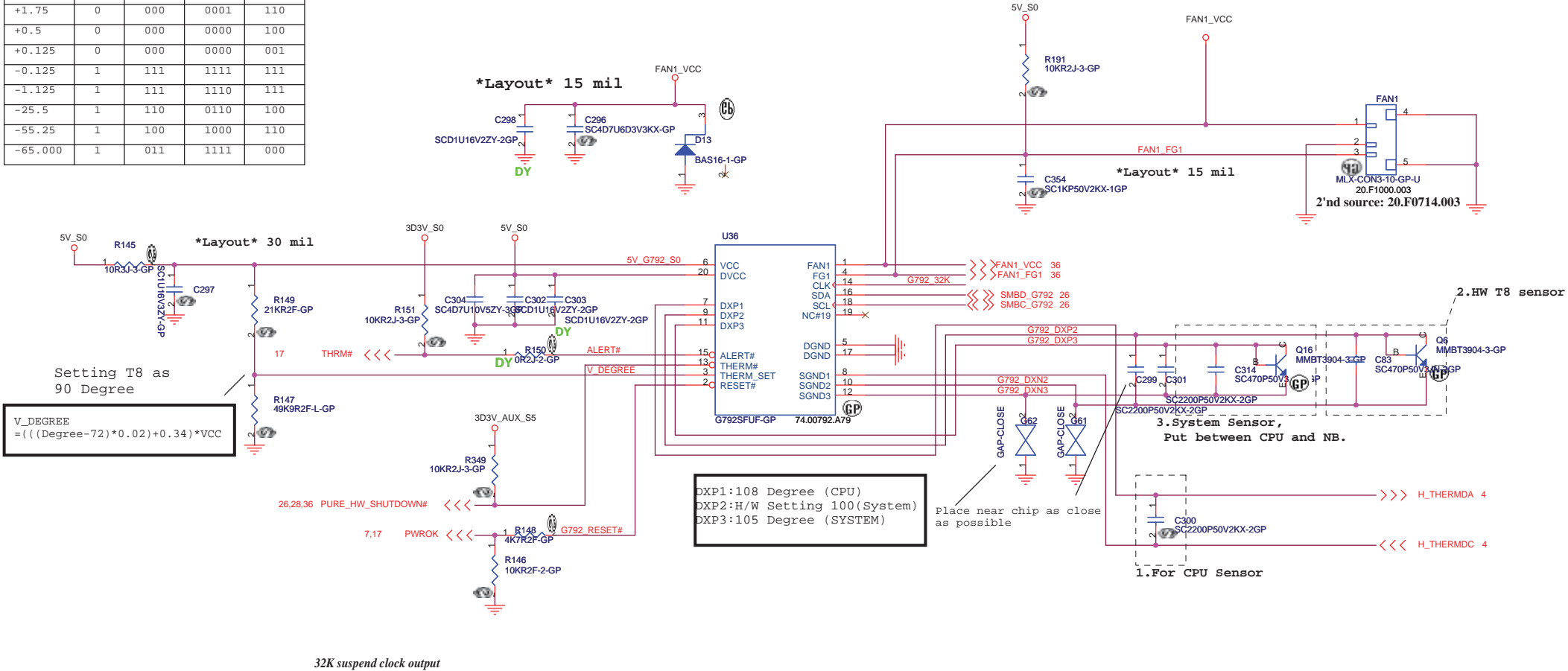




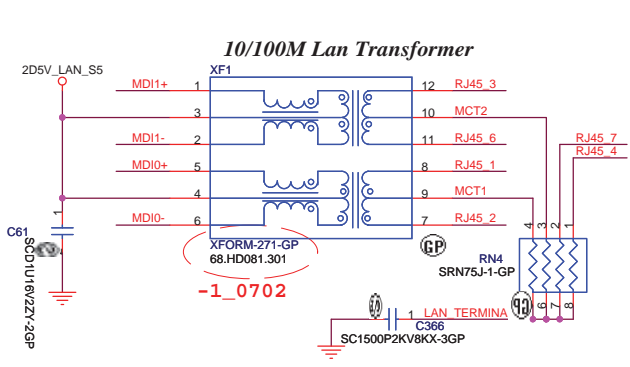
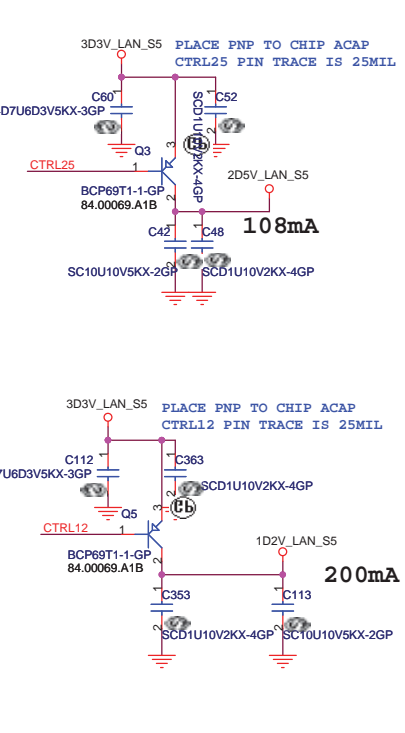
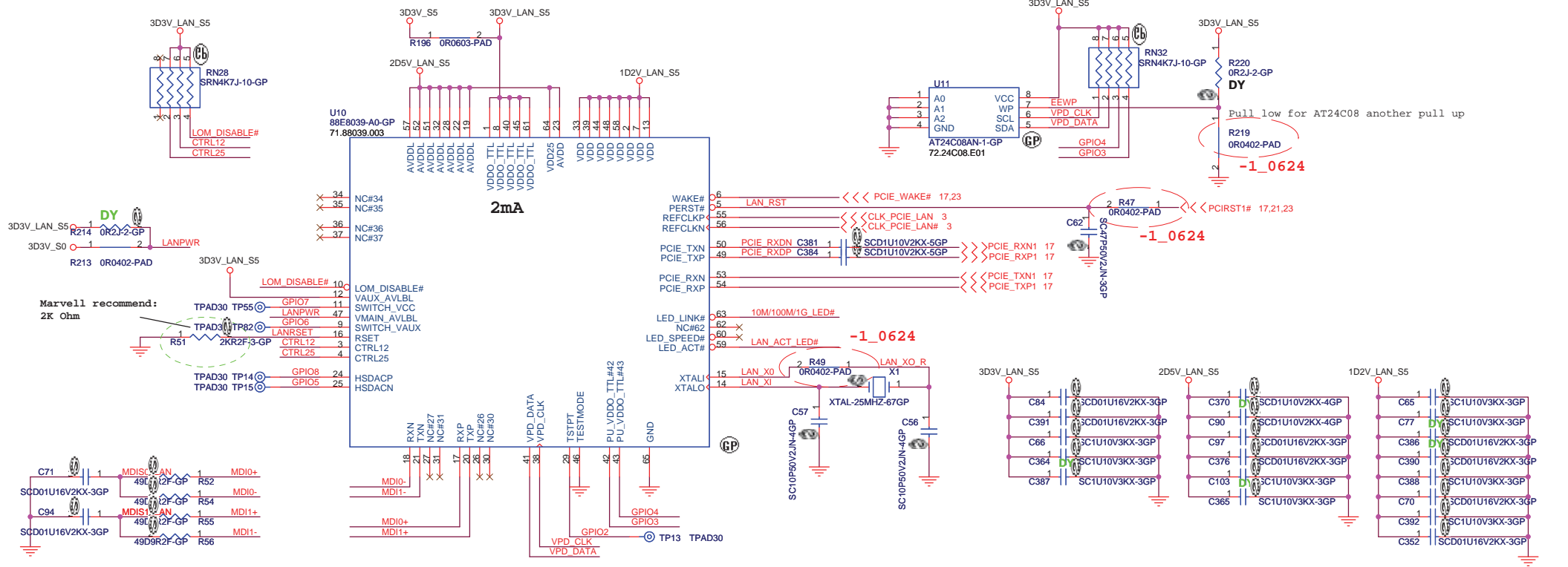


## SMBUS

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000





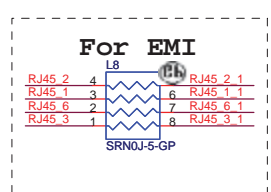


1.route on bottom as differential pairs.  
 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.  
 3.No vias, No 90 degree bends.  
 4.pairs must be equal lengths.  
 5.6mil trace width, 12mil separation.  
 6.36mil between pairs and any other trace.  
 7.Must not cross ground moat, except RJ-45 moat.

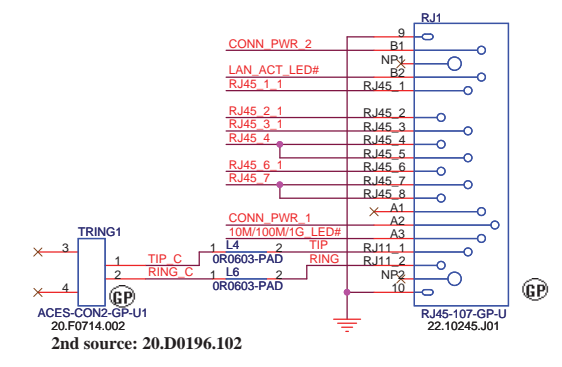
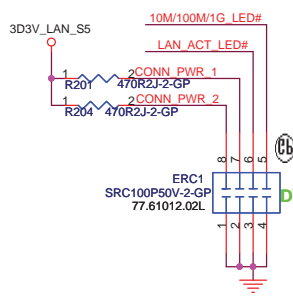
RJ11 signal must leave the other signal or power plane 100mil.

DOC\_TIP, DOC\_RING, TIP\_RING:  
 W/S : 10/100 @ Surface layers  
 10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



36 TIP\_C RING\_C  
 36 RING\_C



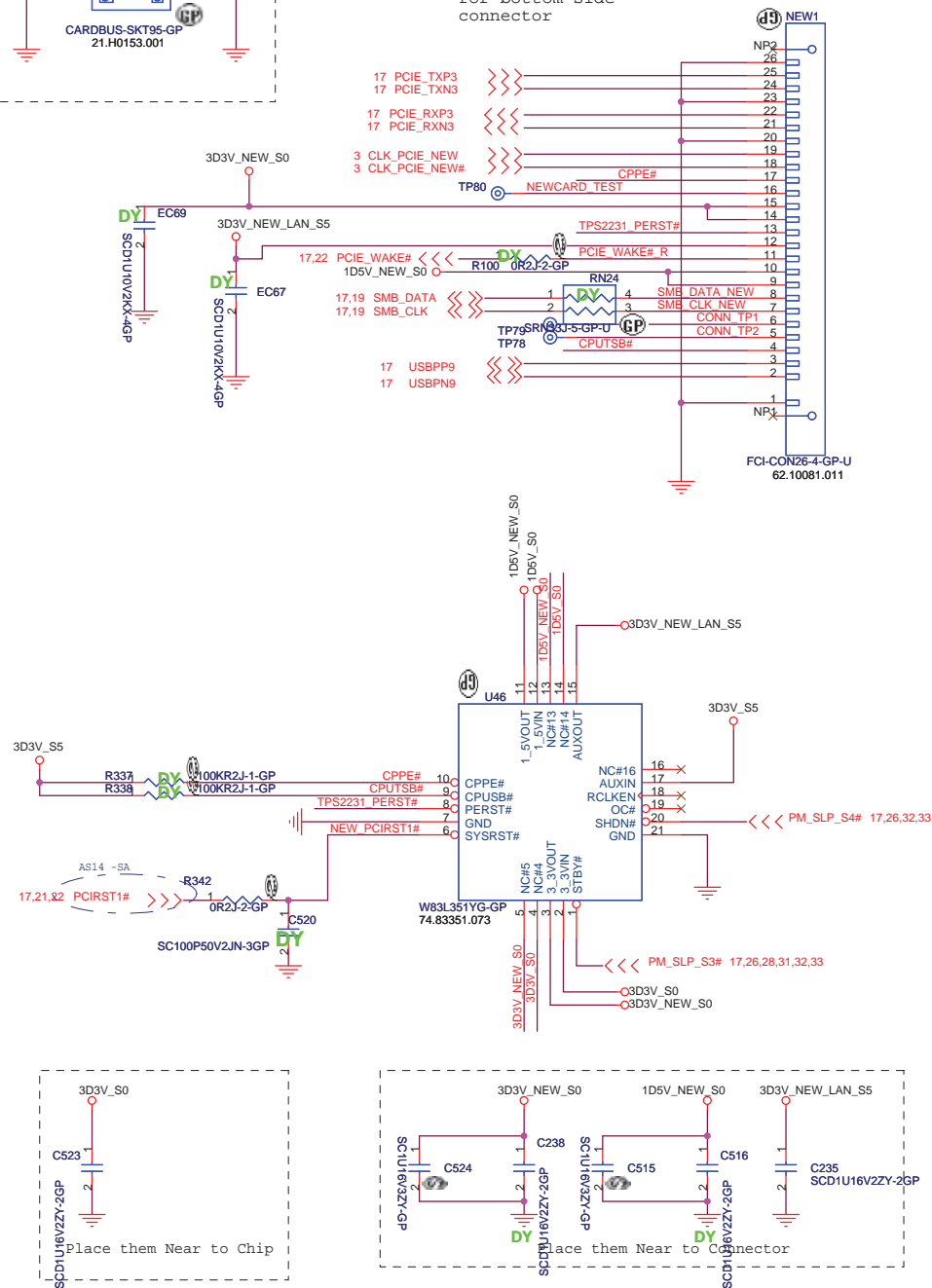
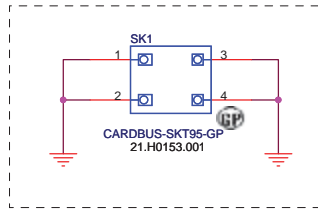
A3:Green  
 B2:YELLOW

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits  
 LAN Data: Yellow(B2), when LAN is transferring data.

RTM

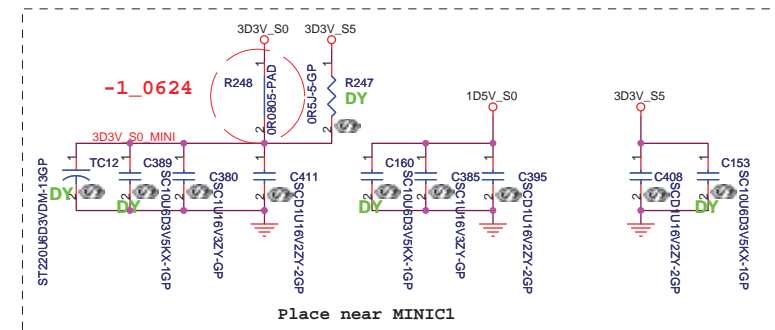
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MARVELL 88E8039</b>	
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Reserve the symbol  
for bottom side  
connector



The schematic diagram illustrates the internal wiring of the Mini-PC board. The central component is the SMT-MINI52P-13-GP module (62.10043.461), which is connected to various power, ground, and signal lines. Key connections include:

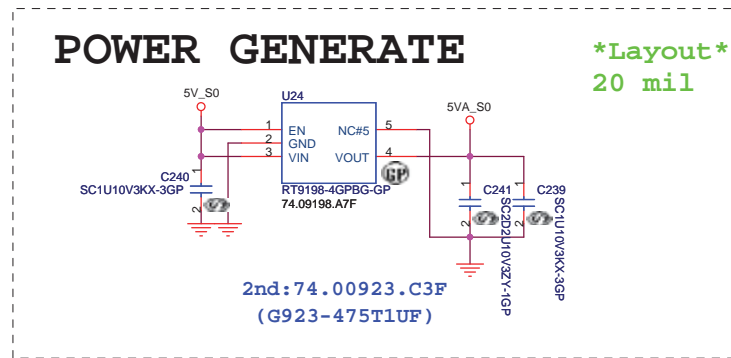
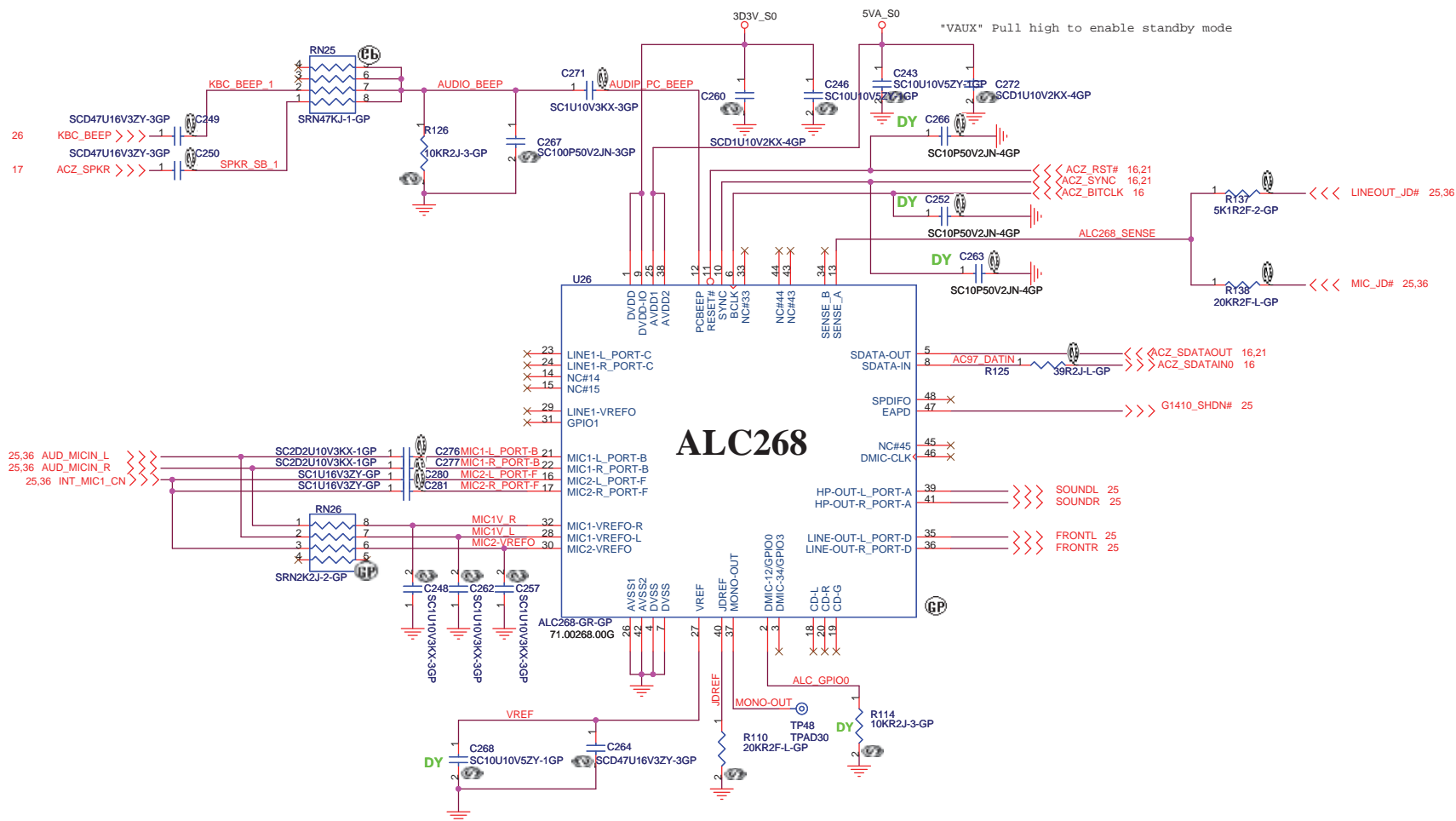
- Power and Ground:**
  - 3D3V\_S0 and 3D3V\_S5 are connected to the module's power pins.
  - 1D5V\_S0 is connected to the module's 5V pin.
  - 5V\_AUX\_S5 MINI is connected to the module's 5V pin.
  - TP20 and TPAD30 are connected to the module's 5V pin.
- Signal and Control:**
  - WIRELESS\_EN (26) and PCIRST1# (17, 21, 22) are connected to the module's signal pins.
  - WLAN\_LED#\_MC (14) is connected to the module's signal pins.
  - USBPN7 and USBPP7 (17) are connected to the module's signal pins.
  - TP12, TPAD28, and TP10, TPAD28 are connected to the module's signal pins.
  - 1LED\_WPAN# and 1LED\_WPAN# are connected to the module's signal pins.
  - CLK\_PCIE\_MINI# (3) and CLK\_PCIE\_MINI# (3) are connected to the module's signal pins.
  - E51\_RxD (26) and E51\_TxD (26) are connected to the module's signal pins.
  - PCIE\_RXN2 (17) and PCIE\_RXP2 (17) are connected to the module's signal pins.
  - PCIE\_TXN2 (17) and PCIE\_TXP2 (17) are connected to the module's signal pins.
  - MINI\_WAKE# (TP20) is connected to the module's signal pins.
- Resistors and Other Components:**
  - R2210 and R222 DY are connected to the module's power pins.
  - DYR225 and 10KR2J-3-GP are connected to the module's signal pins.
  - R208 DY and 0R2J-2-GP are connected to the module's power pins.



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Title			
<b>MINI CARD / NEW CARD</b>			
Size	Document Number	Rev	
	<b>Volvi2</b>	<b>SA</b>	
Date: Thursday, July 05, 2007	Sheet	23	of 36

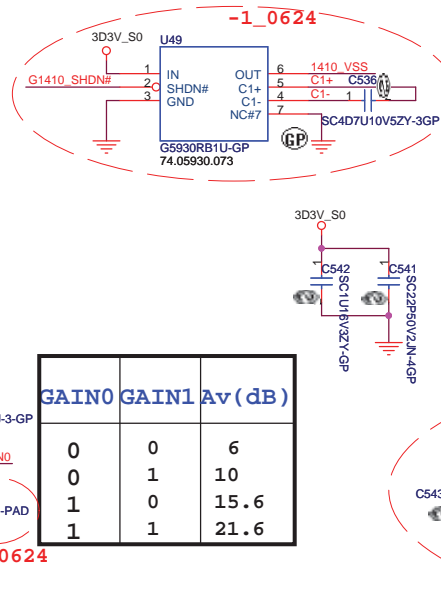
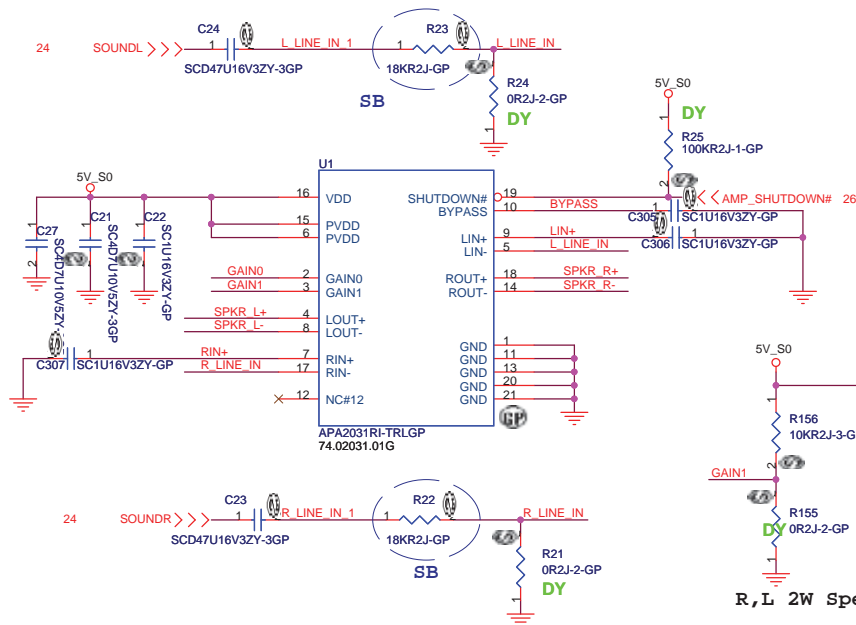




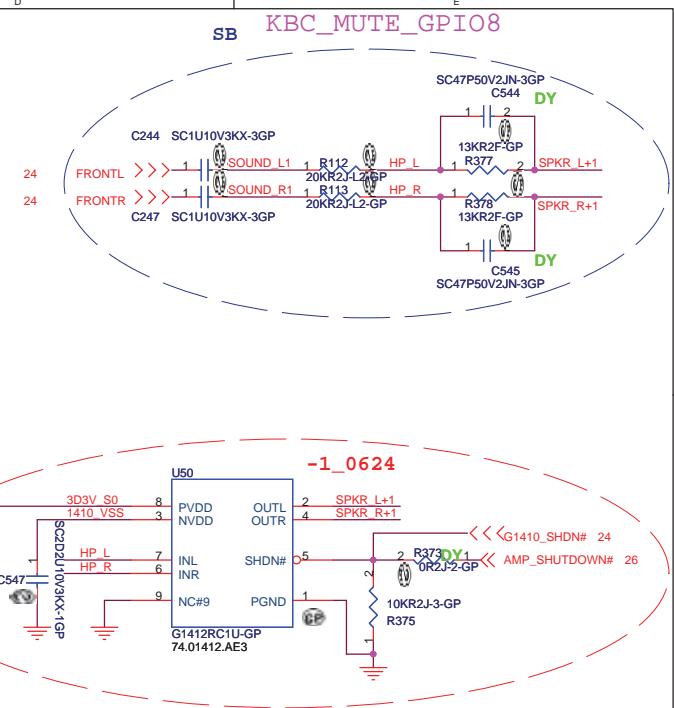
RTM

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Title <b>AZALIA CODEC - ALC268</b>			
Size	Document Number	<b>Volvi2</b>	Rev <b>SA</b>
Date:	Thursday, July 05, 2007	Sheet 24 of	36

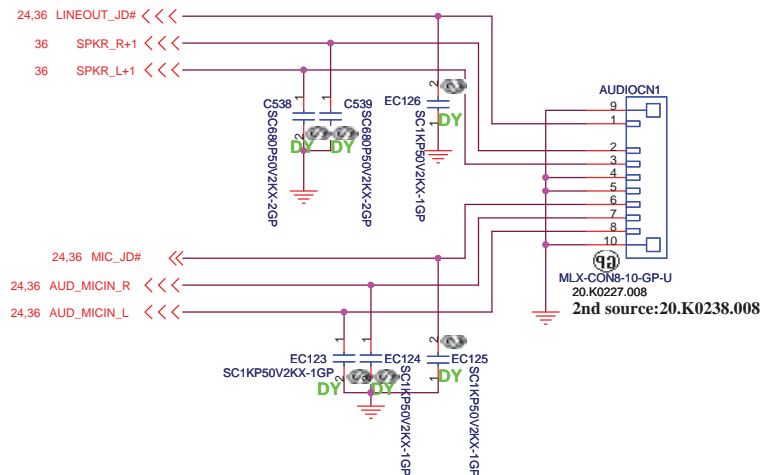
# AUDIO OP AMPLIFIER



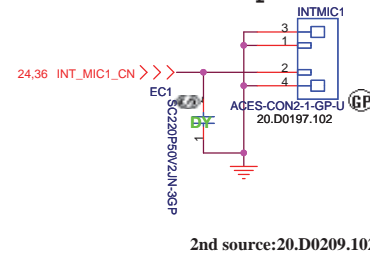
GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6



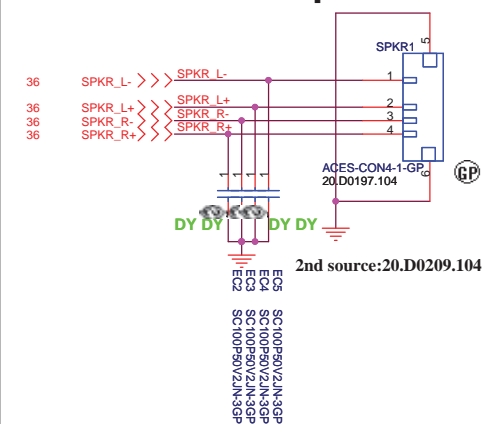
## Audio Connector



## Internal Microphone



## Internal Speaker



RTM

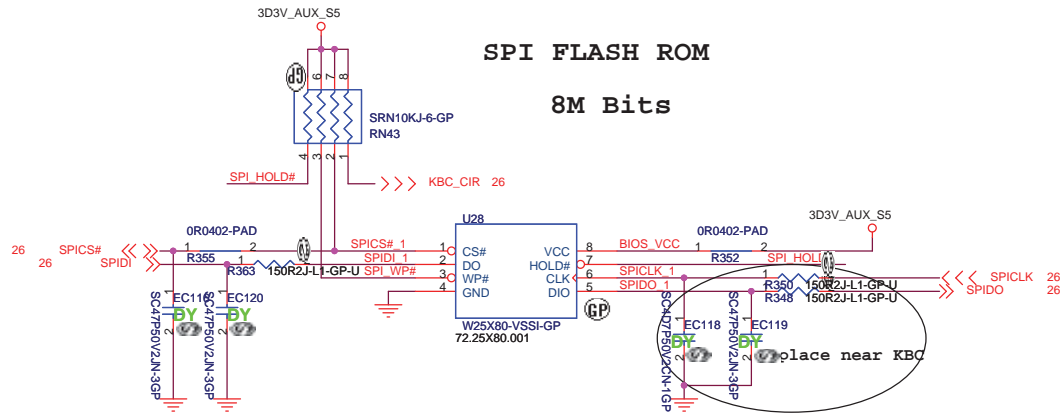
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title  
Size Document Number  
Date: Thursday, July 05, 2007

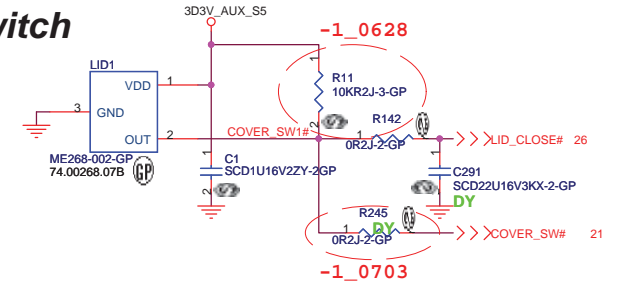
AUDIO AMP AND JACK  
Volvi2  
Sheet 25 of 36

Rev  
-1

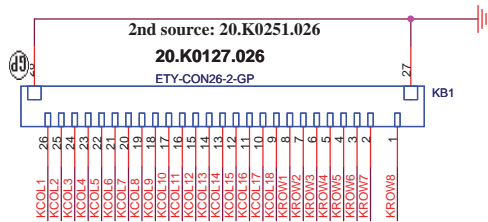
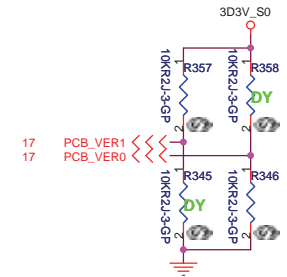




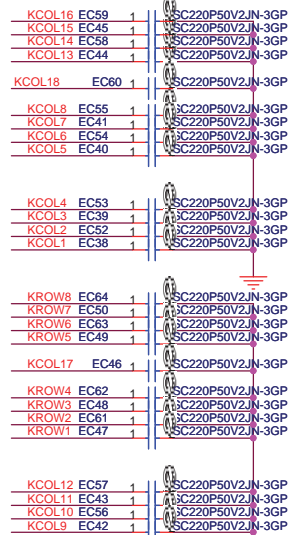
## Hall Switch



PlanarID  
(1,0)  
SA: 0,0  
SB: 0,1  
-1: 1,0  
-2: 1,1



## EMI Bypass cap.



## Internal KeyBoard CONN

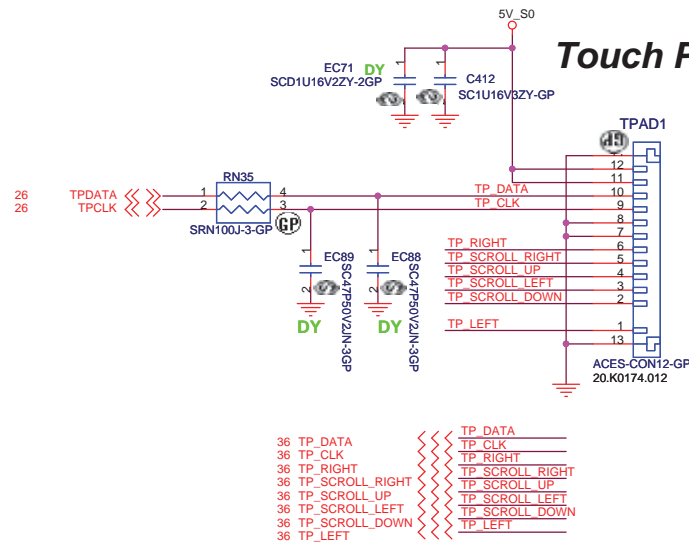
KROW[1..8] >>> KROW[1..8] 26,36

KCOL[1..18] >>> KCOL[1..18] 26,36

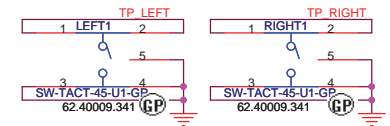


CHECK KB SPEC. AND PIN DEFINE

## Touch Pad CONN



## Touch Pad Button

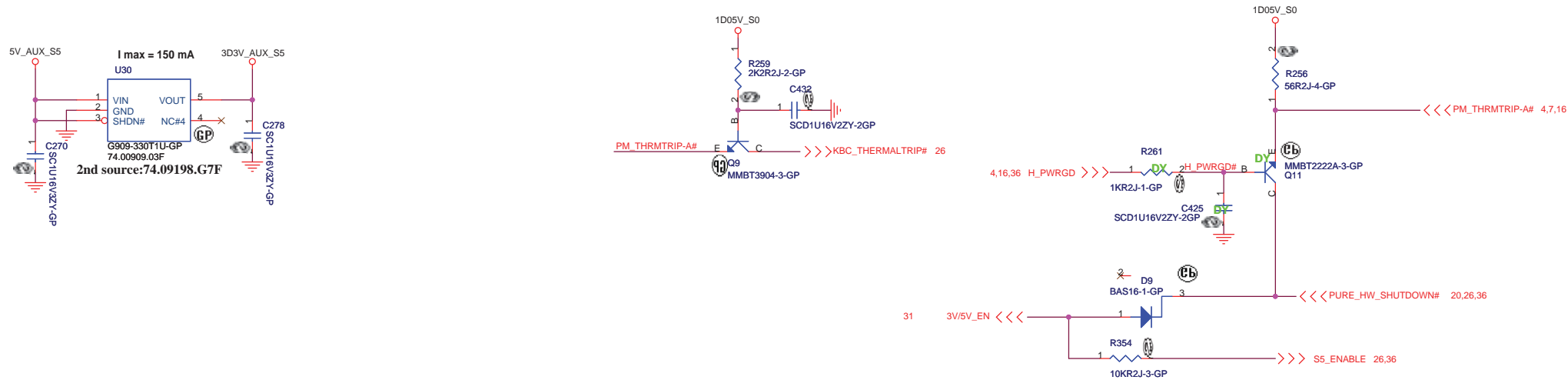


2nd source: 62.40009.431

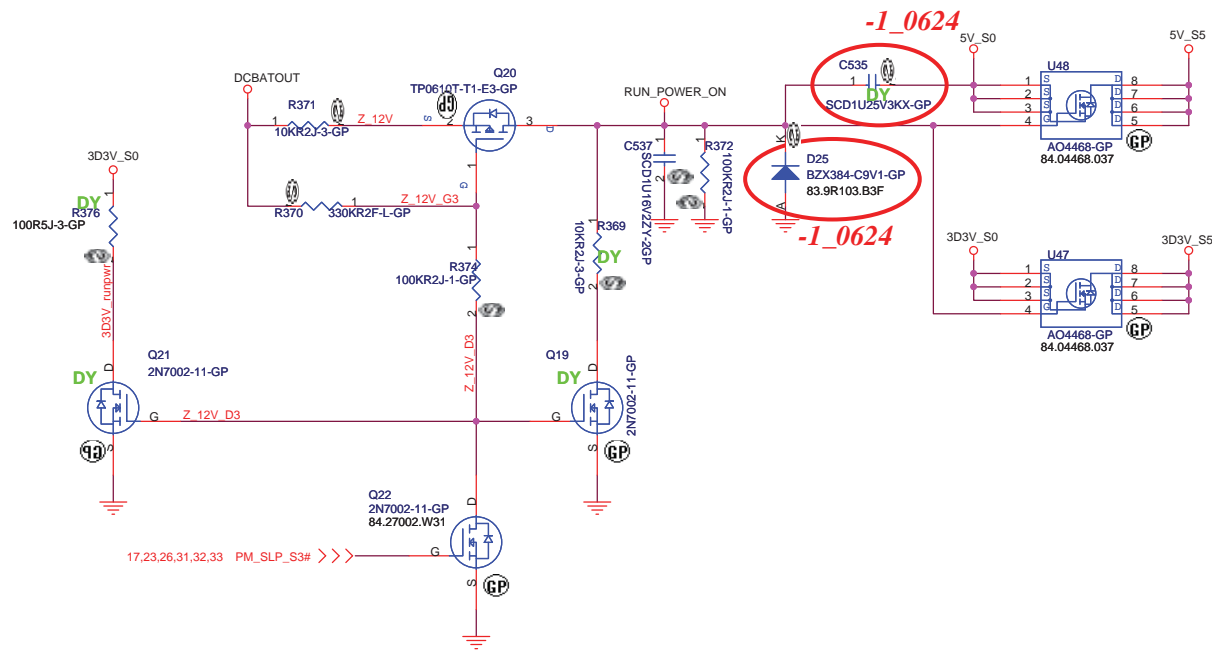
RTM

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Aux Power 3D3V\_AUX\_S5

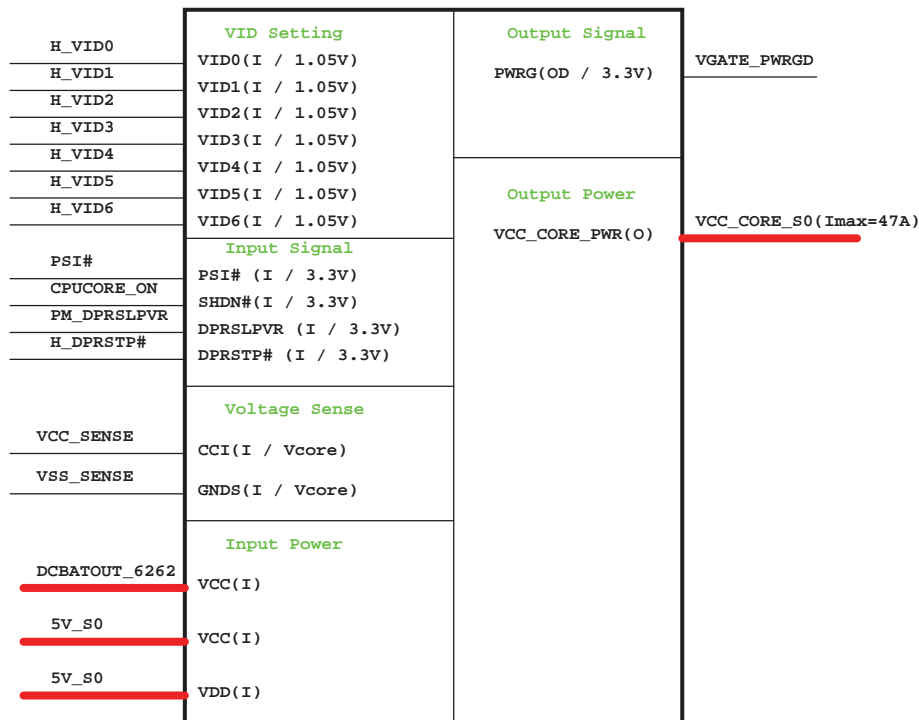


Run Power

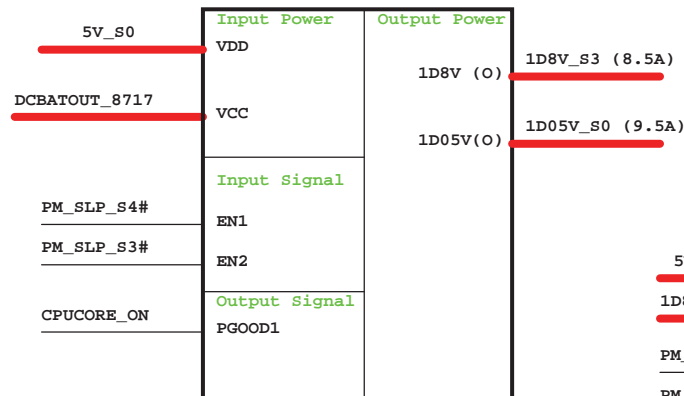




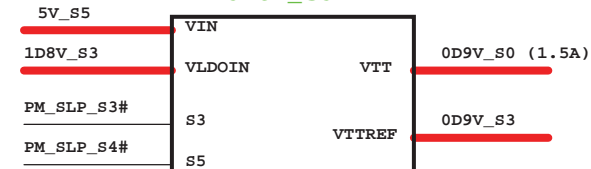
CPU\_CORE  
MAX8770



TPS51124  
1D8V/1D05V

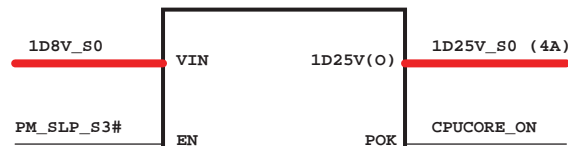


0D9V\_S0



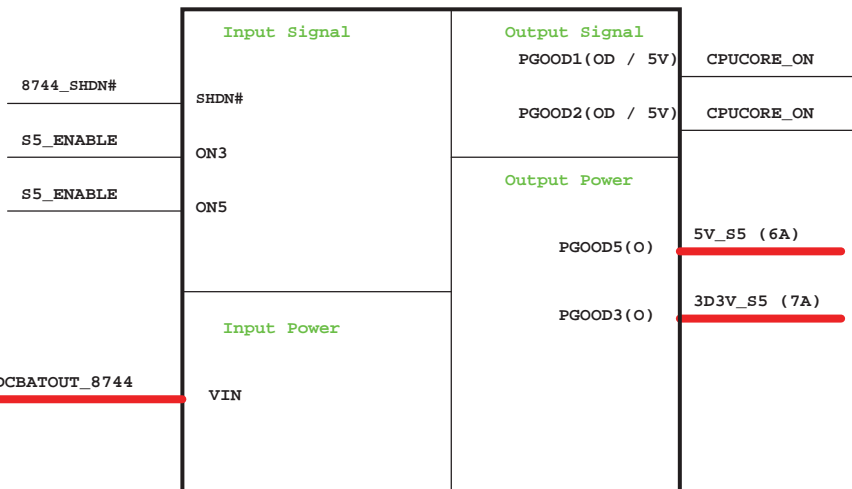
TPS51100

1D25V\_S0

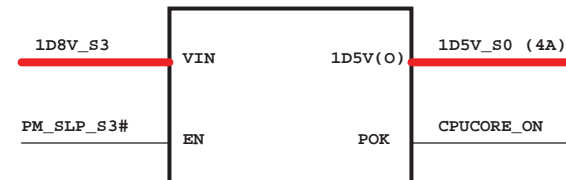


APL5913

MAX8744  
5V/3D3V

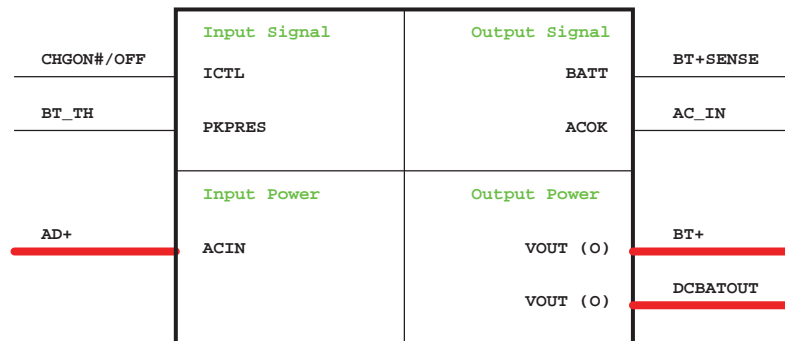


1D5V\_S0



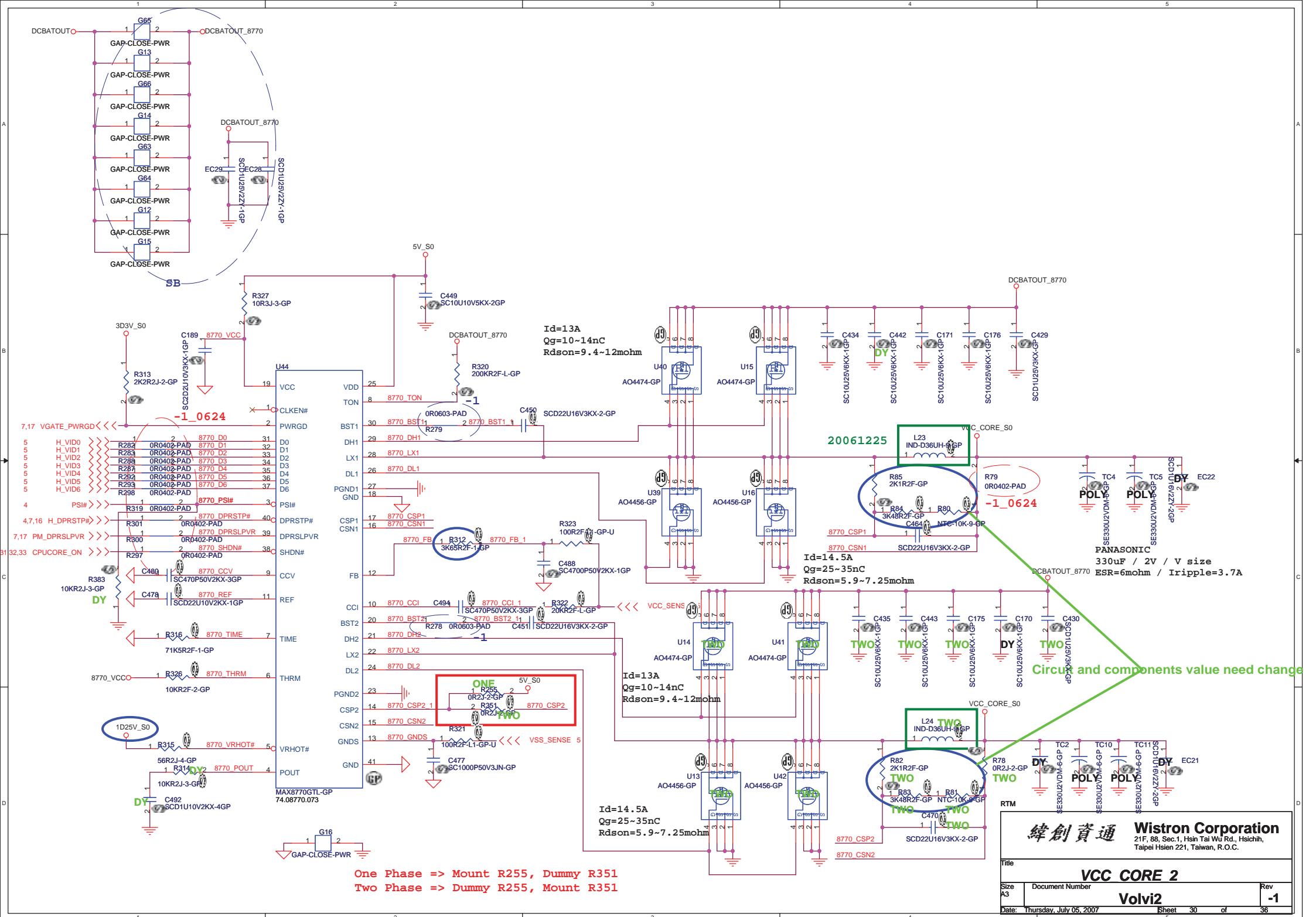
APL5915

Charger MAX8731



RTM

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One Phase => Mount R255, Dummy R351  
Two Phase => Dummy R255, Mount R351

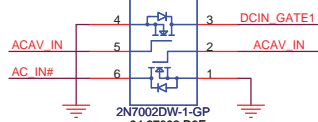
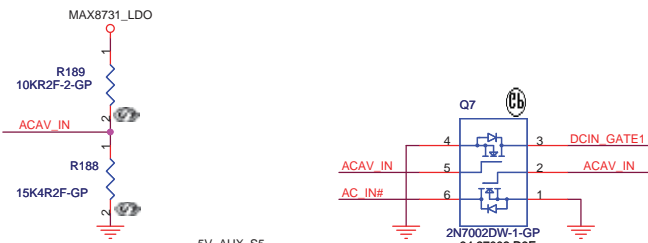
緯創資通 Wistron Corporation  
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Title				
VCC CORE 2				
Size A3	Document Number			Rev -1
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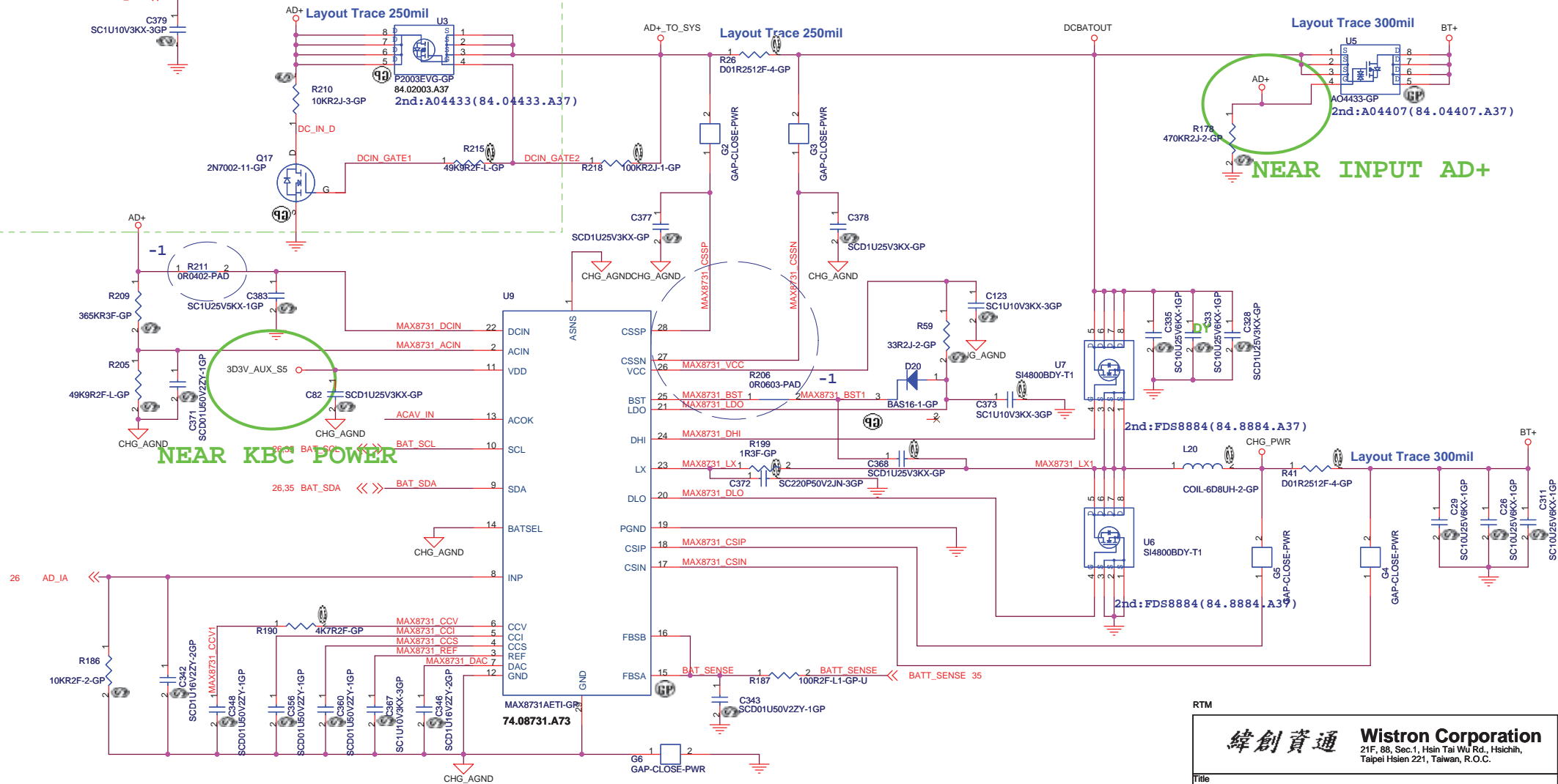






NEAR

## Adaptor In Soft-Start Circuit



Need Check MAXIM Sming Use MAX8731 or MAX8731A

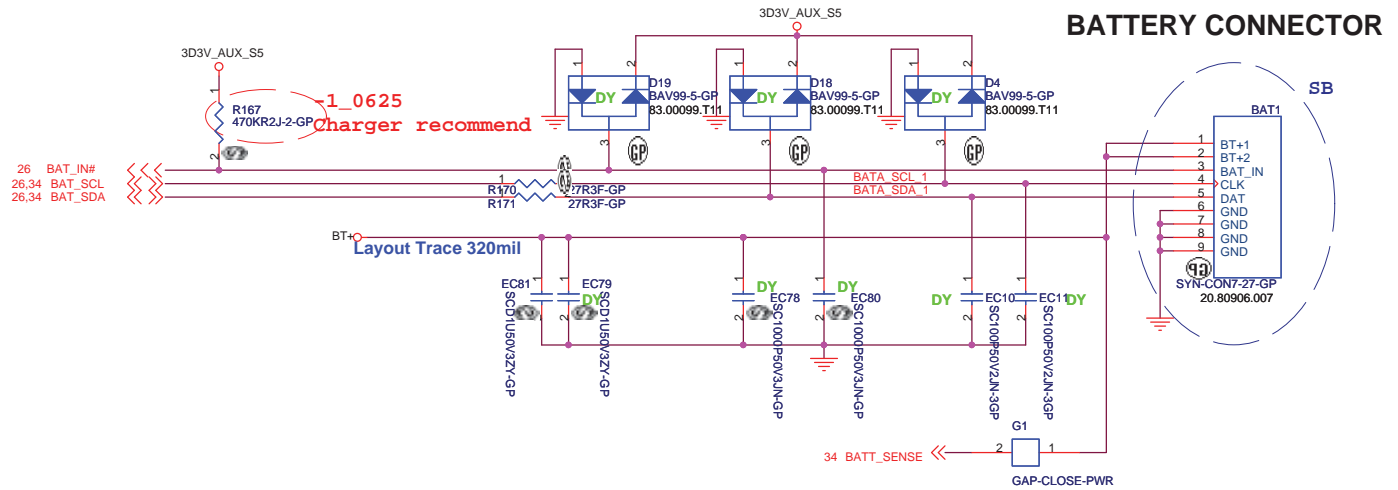
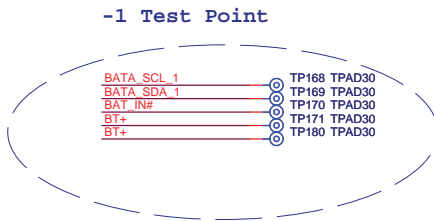
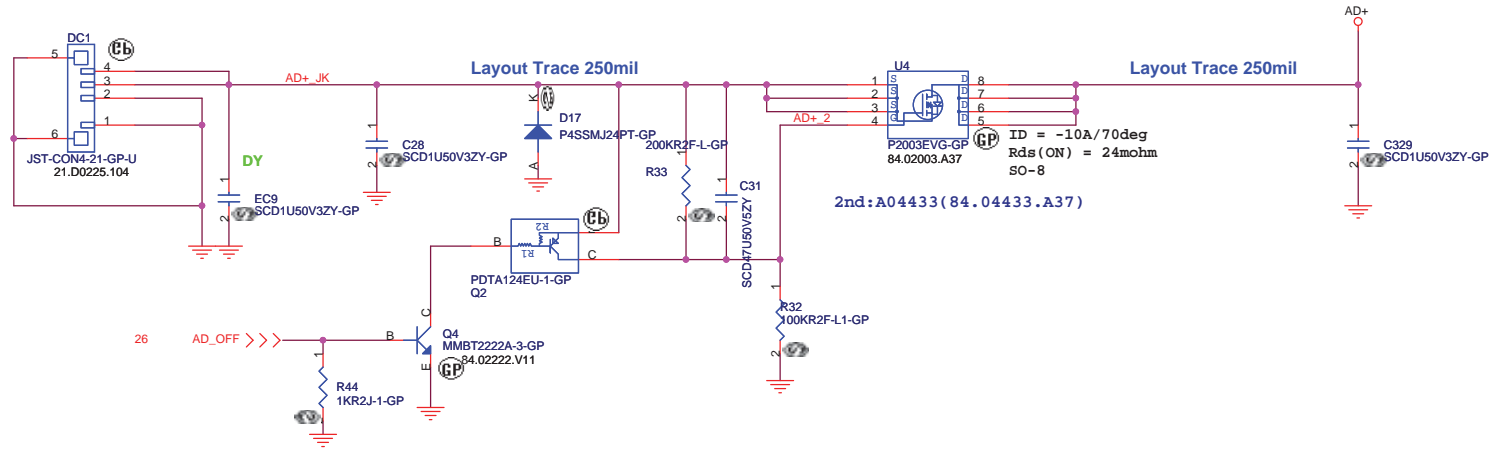
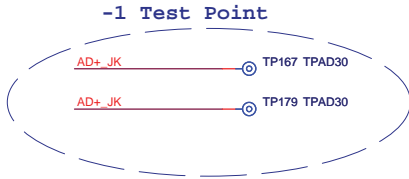
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Title			
CHARGER MAX8731			
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## Adaptor in to generate DCBATOUT



RTM

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Title	Author	Year	Journal	Volume	Page
1. The Effect of Temperature on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2010	Journal of Chemical Education	87	1234
2. Kinetics of the Reaction Between Potassium Dichromate and Hydrogen Peroxide	Jane Smith	2011	Journal of Chemical Education	88	1235
3. The Effect of Concentration on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2012	Journal of Chemical Education	89	1236
4. Kinetics of the Reaction Between Potassium Dichromate and Hydrogen Peroxide	Jane Smith	2013	Journal of Chemical Education	90	1237
5. The Effect of Temperature on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2014	Journal of Chemical Education	91	1238
6. Kinetics of the Reaction Between Potassium Dichromate and Hydrogen Peroxide	Jane Smith	2015	Journal of Chemical Education	92	1239
7. The Effect of Concentration on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2016	Journal of Chemical Education	93	1240
8. Kinetics of the Reaction Between Potassium Dichromate and Hydrogen Peroxide	Jane Smith	2017	Journal of Chemical Education	94	1241
9. The Effect of Temperature on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2018	Journal of Chemical Education	95	1242
10. Kinetics of the Reaction Between Potassium Dichromate and Hydrogen Peroxide	Jane Smith	2019	Journal of Chemical Education	96	1243

**AD/BATT CONN**

Size

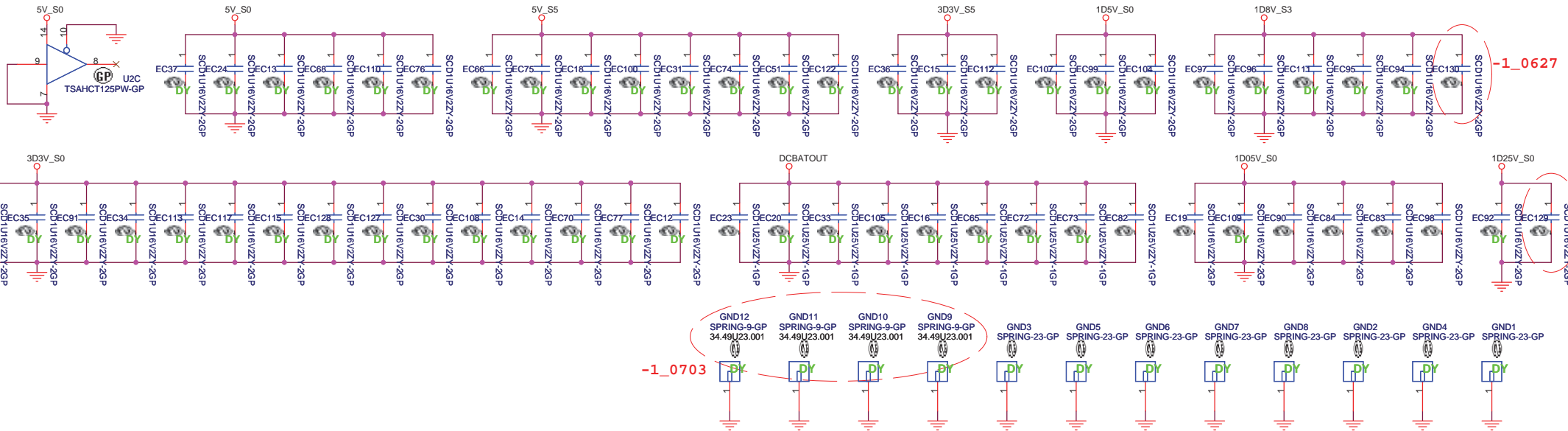
Document Number
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## Volvi2

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3v

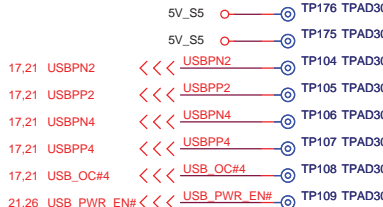


## FAN CONN



## USB ZIF CONN

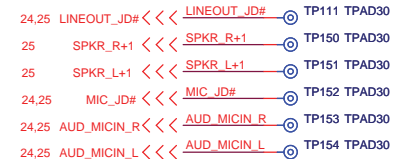
Test Point



## Internal Microphone



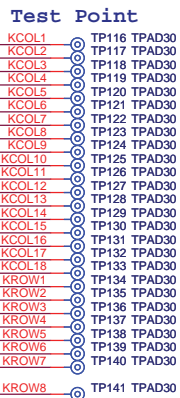
## Audio Connector



## Internal Speaker



## Internal KeyBoard CONN



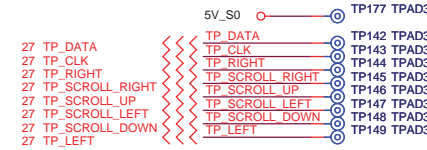
## TRING CONN

Test Point



## Touch Pad CONN

Test Point near TPAD1

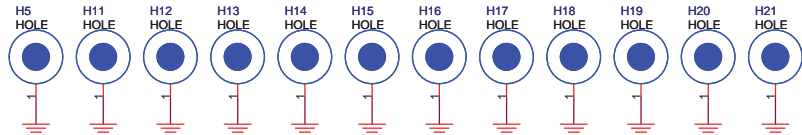
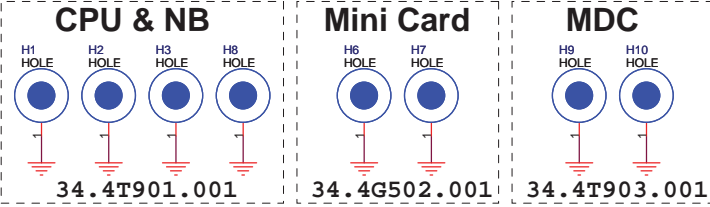


## Check test point



Test Point 放在 Dimm Door 打開可量測處

## STAND OFF ON BOTTOM



RTM

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